PROCEEDINGS OF SCIENCE

CMS Inner Tracker Upgrade

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The LHC is preparing an upgrade, which will bring the luminosity of the machine to 5-7 × 10^{34} $cm^{-2}s^{-1}$ reaching an integrated luminosity of 3000 fb^{-1} by the end of 2037. This High Luminosity LHC (HL-LHC) scenario will require extensive upgrades to the experiments to fully exploit the physics potential of the accelerator. In this so-called Phase-2 upgrade, CMS detector will require improved radiation hardness, higher detector granularity to reduce occupancy, increased bandwidth to accommodate higher data rates, and an improved trigger capability to maintain an acceptable trigger rate. Thus, the entire tracking system will need to be replaced to deal with the HL-LHC environment and to maintain the excellent performance of the current CMS detector.

The Phase-2 Inner Tracker is designed to maintain or even improve the tracking and vertexing capabilities under the high pileup (140 - 200 collisions per bunch crossing) conditions of the HL-LHC. The detectors should have the required radiation tolerance and capability of delivering the desired performance in terms of detector resolution, occupancy, and track separation. The Inner Tracker will be built from thin silicon pixel detectors segmented into pixel sizes of 25 x 100 μm^2 or 50 x 50 μm^2. It is composed of a barrel part with four cylindrical layers and eight small and four large disc-like structures in each forward direction. The design also includes the possibility to extract and replace the degraded parts of the detector without removing the beam pipe. The Tracker Endcap Pixel detector, installed within the extended space, will enable the measurement of real-time instantaneous luminosity as an added functionality. The extended geometrical coverage of up to $\eta < 4.0$ provides large forward acceptance to mitigate the pileup, particularly in the endcap calorimeters.

The 28th International Workshop on Vertex Detectors - Vertex2019
13-18 October, 2019
Lopud, Croatia

PoS(Vertex2019)008

1. Introduction

The instantaneous luminosity of the Large Hadron Collider (LHC) at CERN [1] is continuously raised over time to enhance the sensitivity of the experiments to very rare events and to allow high precision measurements of known processes, e.g. like the properties of the Higgs Boson. A large upgrade project for the LHC, called HL-LHC, is planned and it will bring the instantaneous luminosity of the collider to 5-7 $\times$ 10^{34} $cm^{-2}s^{-1}$ reaching an integrated luminosity of 3000 fb^{-1} by the end of 2037 [2]. At this luminosity, up to 200 simultaneous collisions are generated every 25 ns resulting in around 10 000 charged particles per bunch crossing.

The most extensive upgrade of the accelerator will take place during the years 2025-2027 and it will result in a ten-fold increase in the collision data rate. However, while a high instantaneous luminosity of the accelerator enables a high data recording rate, it also poses significant challenges to the detector systems. Consequently, the LHC experiments need to be upgraded to meet the set goals for high-quality physics data taking.

2. CMS Tracker

The CMS collaboration is currently preparing for the complete refurbishment of the CMS tracking system for the HL-LHC in so-called Phase-2 upgrade taking place in 2025-2027. Like the current Tracker, also the new Tracker will be operated in a 3.8 T magnetic field.

The layout of the Tracker consists of a barrel part complemented by two endcaps. The Tracker barrel part will have ten silicon detector layers [3] as shown in Fig.1. The six outmost layers form the Outer Tracker (OT) and the four innermost ones the Inner Tracker (IT). In OT, the layers from eight to ten (red in the figure) consist of the strip-strip modules and the layers from five to seven (blue in the figure) of strip-pixel modules providing the p_T information in addition to the track position. The barrel part of the Tracker is complemented at larger η by endcap discs. The OT endcap holds five large discs (in figure the strip-pixel modules are marked with blue and the strip-strip modules with red). As illustrated in Fig. 1, the barrel section of the strip-pixel modules is gradually inclined in the range of pseudo-rapidity η between 0.6 and 2.2. The Inner Tracker barrel (TBPX) holds layers one to four and it consists of hybrid silicon pixel modules installed into ladder like structures. The IT endcap holds eight small discs in the forward section (TFPX) with four rings of modules each, and four large discs in the high η extension section (TEPX) with five rings of modules. The measurement of the luminosity will be integrated as additional functionality in the four TEPX discs and the innermost ring of the last TEPX disc will be entirely devoted to the measurement of the bunch-by-bunch luminosity. The IT barrel layers and the endcap rings are illustrated in Fig.1 with green and orange. Green lines correspond to modules made of two readout chips and orange lines represent larger modules with four chips.

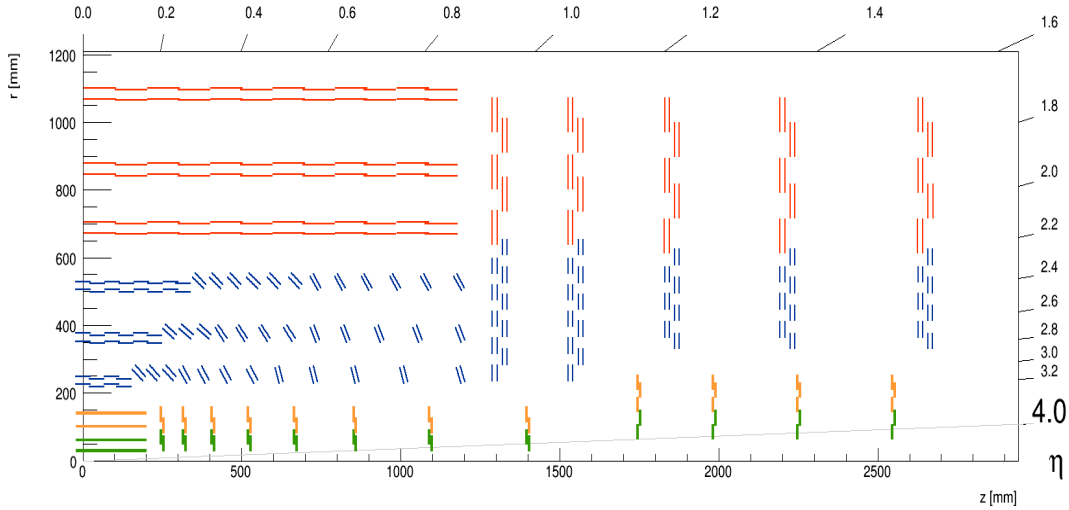

Figure 1.One quarter of the CMS Tracker layout for HL-LHC.

The structure of the Inner Tracker (see Fig. 2) is divided into eight parts to facilitate the installation of the detector inside CMS. It will also allow easier extraction of the detector during the shutdown periods for maintenance and refurbishment of possibly deteriorated parts. The TBPX and TFPX constitute a joint structure installed in four shells. The TEPX will consist of four quarters that will be installed separately. All the IT sections are cooled using a low-mass CO_2-bi-phase cooling with a planned coolant temperature of -35°C circulating in stainless steel pipes and allowing the silicon sensors to be operated below -20°C.

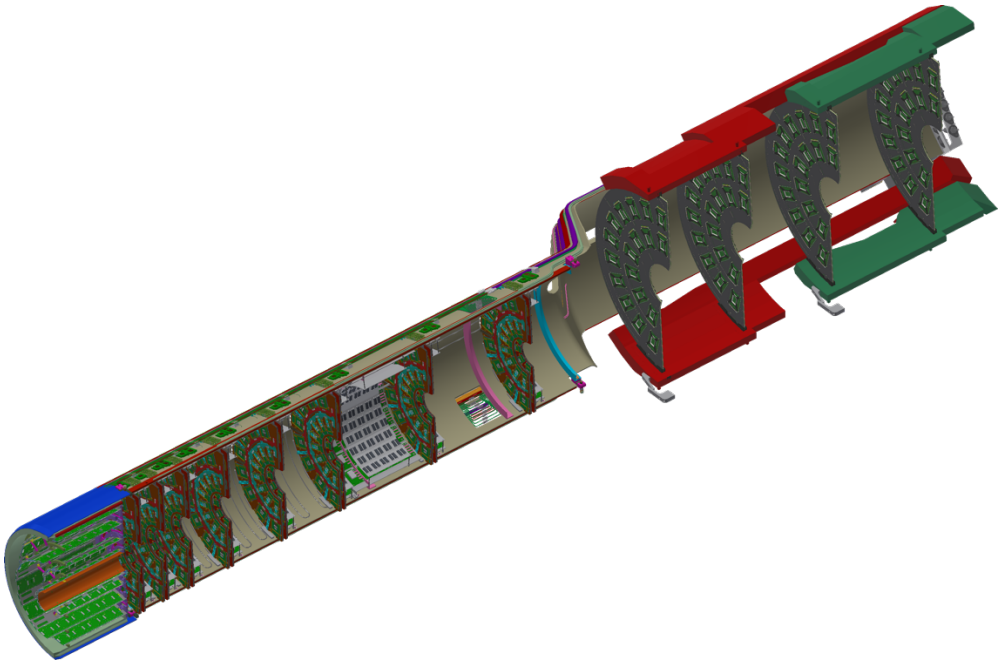

Figure 2. CAD drawing of one quarter of Inner Tracker. showing the TBPX ladders and TFPX and TEPX half-rings (so-called Dees) inside the supporting structures.

3. CMS Inner Tracker system

In the HL-LHC conditions the Inner Tracker will be exposed to radiation levels up to a non-ionizing energy loss equivalent to 2.3×10^{16} n_{eq}/cm^2 and an accumulated total ionizing dose (TID) of 1.2 Grad. Thus, the current Inner Tracker must be replaced with a new detector featuring increased radiation hardness and capability of handling the higher data rate. The new detector will also feature extended pseudo-rapidity η coverage with a tracking volume up to $\eta = 4$.

The CMS Inner Tracker system will cover a total area of 4.9 m^2 with 3892 hybrid silicon detector modules. To increase the modularity and flexibility and to optimize the module production, only two different types of modules are used. Double-chip (1×2) modules are used in the inner layers and rings and quad-chip (2×2) modules on the outer layers and rings (illustrated in Fig.1 with green and orange, respectively).

The inner layers of the IT system are exposed to the harshest radiation environment in the experiment. Thus, the currently ongoing pixel sensor R&D campaign investigates different sensor concepts for the HL-LHC with extensive irradiation and characterization campaigns including test beams in different facilities. The sensors under investigation are 3D and thin (thickness between 100 and 150 µm) n-in-p planar pixel sensors [4][5][6] from different manufacturers, with sensor cell designs of dimensions 25×100 μm^2 and 50×50 μm^2 designed for a readout-chip with 50 µm bump pitch in both directions [3]. The 3D detectors are, however, only investigated as a possible solution for the innermost layer of TBPX and the innermost ring of TFPX.

Initial studies indicate that, in terms of resolution on the track parameters, the relative differences between the 25×100 μm^2 and 50×50 μm^2 designs are typically rather small with a trade-off between primary vertex discrimination and resolution on the impact parameter. At the edges of the barrel layers, and notably for the first layer, square pixels would result in very long clusters, where in each pixel the charge is collected over a path of just above 50 µm, which would set more stringent requirements on the operational threshold of the chip. Moreover, such long clusters would demand a larger bandwidth to read the data out [3]. Possible cell designs for the planar detector case are illustrated in Fig. 3. The narrower pitch increases the density of the pixels by a factor of six with respect to the current CMS pixel detector. The goal is to limit the occupancy below per-mille level [3] and to reduce inefficiencies due to successive hits in the same pixel.

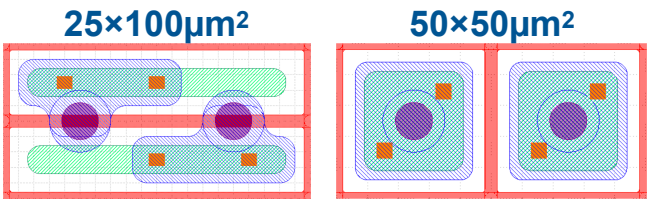

Figure 3. Illustration of IT sensor cell designs of dimensions 25×100 μm^2 (left) and 50×50 μm^2 (right). The p-stop inter-pixel isolation areas are shown in orange, the n-doped implants in green, the metal layer in light purple, the bump pad opening in purple. The orange squares indicate the contact openings.

4. Readout chip

The CERN RD53 collaboration [7] designs and produces the next generation readout chips for the ATLAS and CMS pixel detector upgrades for the HL-LHC. The chips are designed in 65 nm technology, which allows the needed logic density for efficient buffering of the high hit occupancy during long trigger latency.

The first prototype chip, named RD53A, contains an active matrix of 400 × 192 pixels with a cell size of 50 μm × 50 μm. The chip size is 20.0 mm by 11.6 mm, which is about half of the size of the final readout chip. However, the timing and voltage drop requirements are scaled to the final chip size. The RD53A chip is not intended to be a final production readout chip for use in an experiment, and contains design variations for testing purposes [8]. In the chip three different analog front-ends (synchronous, linear and differential) are prototyped in three sub-matrices. The peripheral circuitry is placed at the bottom of the chip and contains all global analog and digital circuitry needed to bias, configure, monitor and readout the chip. The pixel matrix is built of 8 by 8 pixel cores. The 64 front ends within a core are placed as 16 so-called analog islands with four front ends (pixels) each, which are then embedded in a flat digital synthesized "sea" [8] as shown in Fig. 4.

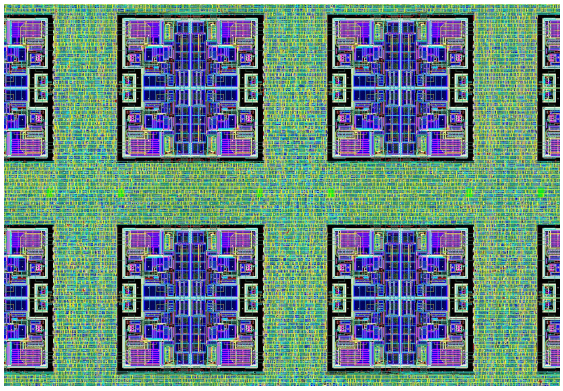

Figure 4. Layout of the analog island concept [8].

The threshold in terms of signal charge at the input is expected to be below 1000 e^-. Test results [9] indicate that all three analog circuitry types can be operated with this upper threshold limit. The required TID tolerance is achieved using dedicated transistor models during synthesis that have been parameterized based on the results from intensive irradiation campaigns described in [10][11]. Very similar results have been obtained from all three sub-matrices. The chip has been proven to be fully functional and meets the specifications up to a TID of 500 Mrad [9]. There are also indications that operation up to 1 Grad would be possible under controlled conditions, most importantly by cooling the chip during the full lifetime.

5.Serial powering

In a conventional detector powering scheme, all readout chips are supplied in parallel with a constant voltage. However, the current consumption of the readout chips results in a voltage drop along the long supply cables and fast current variations result in potentially dangerous voltage transients at the input of the chips. Thus, the amplitude of the tolerable voltage transients combined with the allowed voltage drop defines the needed mass of the cables in the system. The CMS IT for HL-LHC will have 13488 pixel readout chips [3] with a maximum supply current of about 2 A per chip. It has been calculated that the needed power is in the order of 50 kW. If this power was to be provided by conventional methods, and minimizing the power losses in the cables, it would translate into about six tons of cables and therefore, a significant amount of material in the path of the particles to be detected. Thus, a different power scheme had to be found for the HL-LHC era.

One possible solution is to develop a system with constant current consumption. In this, so-called serial powering concept, a chain of modules is powered in series by a constant current [12]. Thus, only two power lines per chain are needed. The concept offers a drastic reduction in the amount of power lines in the active region of the detector thus minimizing the power losses and heat generation on the power lines. The concept also minimizes the transients by design and therefore the cable mass does not depend on the supply current and tolerable voltage transients. The needed supply current can be further reduced when the supply current delivered to a chip is re-used. In CMS IT the modules are connected in chains of up to eleven modules [3]. A controlled splitting of the supply current between the chips on the module (connected in parallel) is needed and achieved by dedicated Shunt-LDO regulator blocks implemented in the readout chip [13]. The upgraded ATLAS [14] and CMS pixel detectors for HL-LHC are the first large scale applications of the serial powering in a tracking detector system.

6. Modules and mechanics

The pixel module design is based on hybrid technology, where the pixel sensor is flip-chip bonded to the readout chips, which are wire-bonded to the so-called High-Density Interconnection (HDI) boards [3]. The chips are placed in a 1 × 2 (one row, two columns) or in a 2 × 2 (two rows, two columns) arrangement (see Fig. 5) and the HDI board is glued on top of the sensor. The HDI boards are used for distributing signals and power to and from the pixel modules. In the module, the readout chip is the only active component making the modules very simple and robust. Only a few passive components, mostly decoupling capacitors and connectors, are hosted on the HDI. Each module will have dedicated readout links (described in Sect. 7.) and a serial power connection, which is used between adjacent modules to feed the current to the next module in the chain. The largest challenges for the HDI design are the current return paths, high voltage operation up to 1000 V and the low material budget.

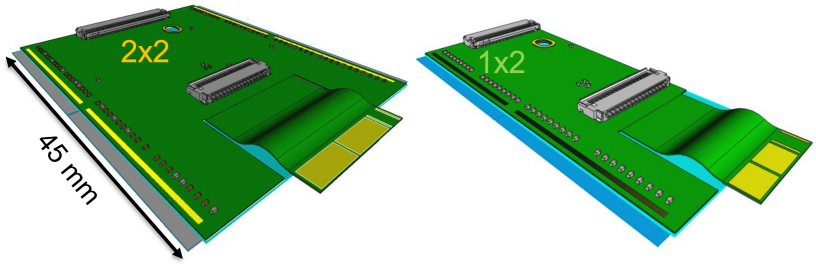

Figure 5. CAD *drawing of the two different IT module flavors.*

The mechanical support structure for the IT upgrade has not been finalized yet, but is under constant improvement to optimize it for the HL-LHC. For the TBPX a lightweight carbon ladder structure like in the Phase 1 pixel detector [15] is being designed. For the TFPX and TEPX, half-disc structures consisting of carbon foam and carbon laminates are investigated.

7. High-speed electrical links and optoboards

In the Inner Tracker, the bidirectional data transfer to achieve the needed bandwidth to allow data acquisition (DAQ) at higher data rates is implemented using lows-mass high-speed electrical links (e-links) [16]. The data readout links will be running at 1.28 Gbps with the Aurora protocol [17], while the control links will be running at 160 Mbps with a custom protocol. These e-links will be as short and as light as possible (maximum length about 1 m) and they will connect the pixel modules to the optoboards. In addition, the electrical links need to be AC-coupled, as due to the serial powering concept, the local grounds along the module chain can be different. Special protocols with DC-balanced symbols, such as the Aurora, have been chosen exactly for this reason and they are combined with decoupling capacitors close to the receiver side.

A Low-Power GigaBitTransceiver (LpGBT) chip supports up to 7 readout links at 1.28 Gbps and 8 control links at 160 Mbps [18]. The chip has data aggregation capability, enabling the implementation of multiple links per chip or aggregating 2 or 4 chips of a module into a single link thus offering the possibility to adapt the density of e-links to the data rates expected in the different parts of the detector. In the current IT layout, in the innermost layer up to 6 links per module can be used, whereas on the outer layers of the detector a single link is expected to be sufficient. For the control, one control link per module us used. Altogether, for the entire IT system, 10800 e-links will be used to readout and control 3892 pixel modules with 778 optoboards.

The optoboards host the LpGBT chips and the Versatile Links (VL+). On the optoboards the electrical data signals received from the detector are multiplexed and converted into optical signals at 10 Gbps rate. The optoboard is powered by a pair of DC-DC converters providing power to two LpGBT chips and two VL+ links. As the optoboards have only a limited radiation tolerance (a maximum total dose of 100 Mrad and fluence of 3×15 n_{eq}/cm^2), they cannot be placed on the pixel modules, but have to be installed further from the collision point, which necessitates the use

of the e-links. For the TFPX and TEPX, the location will be at the periphery of the ring structures, while for the barrel, there are three potential locations at the higher radii from the collision point.

8.Trigger and Control Board

The optical links on the on-detector optoboards send out the data to the back-end electronics, as described in the previous section and illustrated in Fig. 6. Readout links are carrying data from events accepted by the first trigger-stage and monitoring information to the DAQ and control system, and control links (shown in pink and red arrows) are used to send clock, trigger, and configuration commands to the pixel modules. A dedicated IT DAQ Interface board called DTC (Data, Trigger and Control) sends and receives data from the detector modules. This board is a custom developed ATCA (Advanced Telecom Computer Architecture) blade based on commercial FPGAs and multi-channel optoelectronic transceivers [3]. Each DTC has two "half-DTC" FPGAs that can receive up to 36 optical fibers. Altogether, 28 DTCs will be needed to readout the entire IT. The data and control signal paths between the modules and the DAQ are shown in Fig. 6.

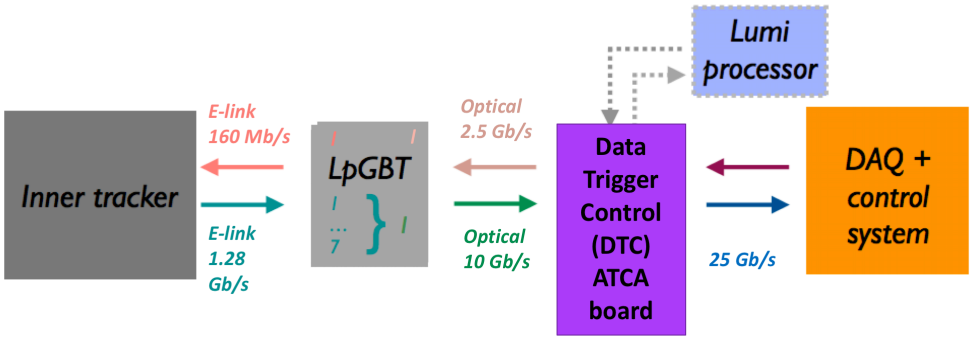

Figure 6. Schematics of the off-detector electronics describing the paths of data and control signals between the IT modules and DAQ.

9.Conclusions

In the HL-LHC era the CMS IT will require improved radiation hardness, higher detector granularity to reduce occupancy, and increased bandwidth to accommodate higher data rates. A large number of technical challenges will thus need to be overcome by 2027 to be able to benefit from the 10 times higher luminosity of the HL-LHC. Several novel solutions have been developed to address the challenges and to achieve a detector with efficient power distribution and low material budget. Significant progress has been made in the detector development, but there are still critical decisions to be made for the detector design and optimizing it for the high occupancy environment. For that the year 2020 will be important as the final readout chip will be submitted for production and the chips will become available for prototyping work.

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