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The LHCb Upstream Tracker Upgrade

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The LHCb experiment is a forward spectrometer at the Large Hadron Collider designed to study the decays of beauty and charm hadrons. During the recently concluded data taking, it produced a vast amount of data, in flavor physics and in additional physics topics that take advantage of the forward acceptance of the LHCb experiment. In the LHC's second long shutdown, a major upgrade of the LHCb detector is being installed and commissioned. The upgraded detector will take data at higher luminosity and will implement a flexible software trigger that requires all the detector components to push out their information at 40 MHz. The Upstream Tracker is a new silicon strip detector placed upstream of the LHCb bending magnet, composed of four planes of silicon microstrip detectors mounted on both sides of vertical structures called staves, providing mechanical support and CO_2 evaporative cooling. Four different silicon sensor designs are used to handle the varying occupancy over the detector acceptance. A dedicated front-end ASIC, the SALT chip, provides pulse shaping with fast baseline restoration, digitization via 6-bit ADCs, and digital signal processing providing pedestal and common-mode noise subtraction as well as zero-suppression. Near detector electronics implements the transformation to optical signals that are transmitted to the remote data acquisition system and regulates low-voltage power distribution. In this contribution, the performance of the individual detector components is reviewed, with particular emphasis on studies of the sensor-SALT hybrid modules and instrumented staves.

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1. Introduction

The LHCb experiment is a general purpose forward spectrometer located at the Large Hadron Collider (LHC). The experiment is focused on studies of the decays of beauty and charm hadrons, but also studies a wide range of physics using its unique forward geometry. After the end of LHC data taking in 2018, a shutdown period is ongoing until 2021. During this long shutdown, the LHCb experiment is installing a major upgrade to the detector [1]. When data taking resumes, it is expected that the collision luminosity at the LHCb interaction point will increase from $4 \times 10^{32}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ to $2 \times 10^{33}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. To make the most of this increase, LHCb will read out all components of the detector at the collision rate of 40 MHz, and make all trigger decisions in software. The main challenge for new detector components is thus to allow this fast readout while coping with increased occupancy and maintaining or improving the excellent performance of the detector in earlier runs.

As part of this upgrade, the three main tracking detector components of LHCb are all being replaced; the new detectors are the Vertex Locator (VELO), Upstream Tracker (UT), and Scintillating Fiber Tracker (SciFi) [2, 3]. The UT is a silicon microstrip detector located just before the dipole bending magnet, as shown in fig. 1. The UT plays an important role in the software trigger. Requiring that a particle is detected in the UT in addition to the VELO and SciFi greatly reduces the number of possible track segment combinations which greatly reduces the amount of fake (or "ghost") tracks and increases the processing rate in the trigger. Processing rate is also improved by making a momentum measurement using VELO and UT before the bending magnet, which narrows the search windows in the SciFi. For this reason the most important goal for the UT is to be highly efficient for track detection with no dead areas and as large an acceptance as possible.

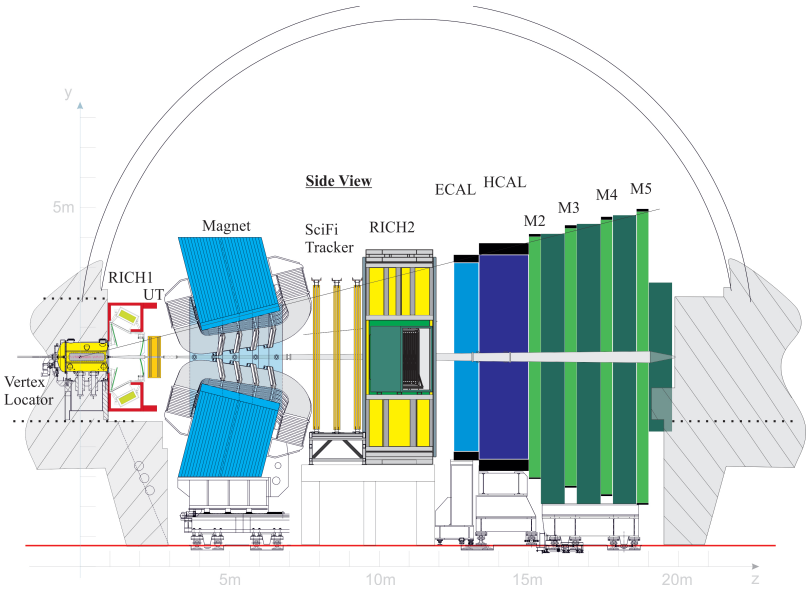


Figure 1: Side-view layout of the LHCb upgrade. Collisions occur inside the Vertex Locator. The Upstream Tracker (UT) is located just before the dipole bending magnet. From Ref. [3].

2. UT components

The UT sensitive area is composed of about 1000 silicon microstrip sensors making up four tracking planes as pictured in fig. 2. The middle two layers are placed at stereo angles of 5°. Four different sensor designs are used to increase acceptance and to cope with high occupancy in the central region of the detector around the beam pipe. The sensors are arranged to have no insensitive gaps inside the detector acceptance. The sensors have been manufactured by Hamamatsu Photonics.

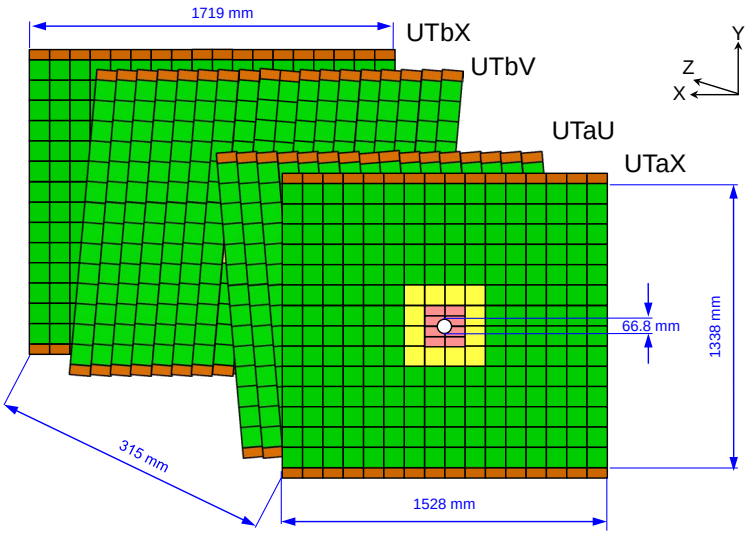
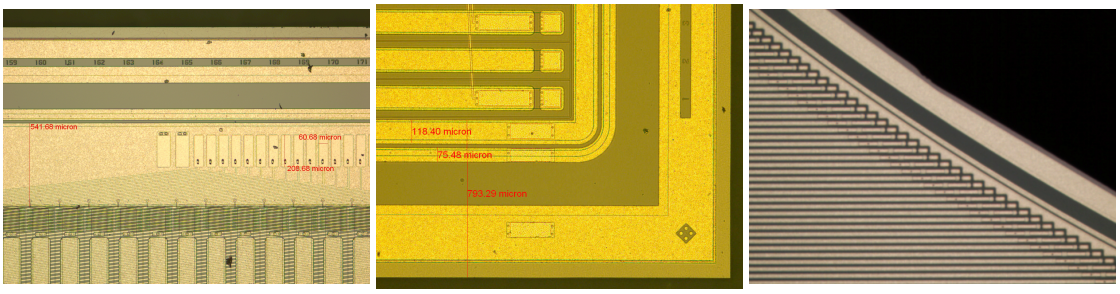


Figure 2: Layout of the silicon sensors making up the UT. The green rectangles represent Type A sensors. Type B sensors are shown in yellow, with Types C and D in pink. From Ref. [3].

The majority of the sensors, making up the regions away from the beam pipe, are referred to as Type A. These are approximately 10 cm by 10 cm, 320 µm thick p-on-n sensors with 512 strips at a pitch of 187.5 µm. To match the pitch of the readout electronics, these sensors include an embedded pitch adapter in an additional metal layer near the edge of the active area. A picture of part of this pitch adapter is shown in fig. 3a. Bias voltage is applied to the sensors via a top-side contact connected to a floating cathode implant around the edge of the sensor shown in fig. 3b. An extensive test beam campaign has demonstrated that these features perform well, even after irradiation to the maximum fluences expected [4, 5, 6, 7].

The remaining sensors nearer the beam (Types B, C, and D) must cope with the increased occupancy by increased segmentation. They are all n-on-p silicon sensors with 1024 strips at a pitch of 93.5 µm. The Type B sensors are 320 µm thick like the A, while the Type C and D are 250 µm thick. The Type C and D sensors have a length parallel to the strips of approximately 5 cm. To increase acceptance for particles at small angles to the beam, the Type D sensors have a circular "cut-out" with a radius of 34 mm in one corner, shown in fig. 3c.

The sensors are constructed into modules by connecting them to a hybrid flex circuit supporting either four or eight SALT readout Application Specific Integrated Circuits (ASICs) [8], depending on the number of sensor strips. The hybrid has four metal layers with a total thickness



(a) Embedded pitch-adapter (b) Top-side HV contact (c) Type-D cut-out

Figure 3: Principle design features of the UT silicon sensors. The Type A sensors include an embedded pitch-adapter (a) to match the readout electronics pitch. All sensor types are biased via a high voltage contact on the front side of the sensor which is visible in (b) as the rectangular contact on the metal layer which runs around the outside edge of the sensor. The Type D sensors feature a circular cut-out with a radius of 34 mm to accommodate the beam pipe, the curved edge of which is shown in (c).

of about 280 µm. The first module constructed from production components is shown in fig. 4. Signals from the sensors are read out and processed by the SALT,which can read out 128 channels at 40 MHz with a fast return to baseline. It includes a 6-bit ADC and digital signal processing; a block diagram is shown in fig. 5. The digital processing allows for common mode noise and pedestal subtraction and zero suppression. The SALT has gone through a number of revisions leading up to the current v3. The most serious issue involved large oscillations in the baseline when using multiple ASICs together in a module; this can be visualized as huge jumps in the common mode as shown in fig. 6a. In v3, this oscillation is under control, as seen in the pulse shape of fig. 6b which was measured from a hybrid test with four SALT chips active. The pulse shape is measured by scanning the ADC sampling time over the range depicted. During system operation this pulse will be sampled at a specific time close to the peak to measure the output. There is a visible 40 MHz ripple in this measurement for all times; this is a fixed pattern and does not represent noise in the system. For the signal to noise ratio in the final system, we expect results in the range of 12 to 15.

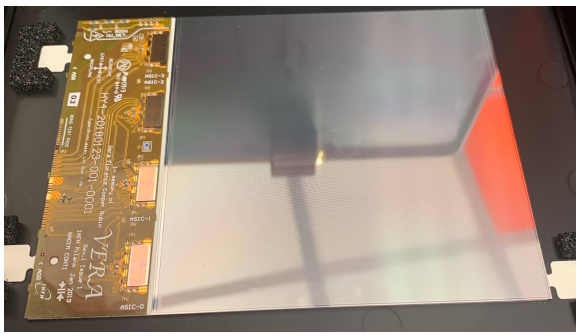


Figure 4: First module with production sensor, hybrid circuit, and ASICs.

The modules are supported in the detector by a number of vertical staves which are mounted side-by-side in the detector box as shown in fig. 7a to create the layers. The staves are constructed

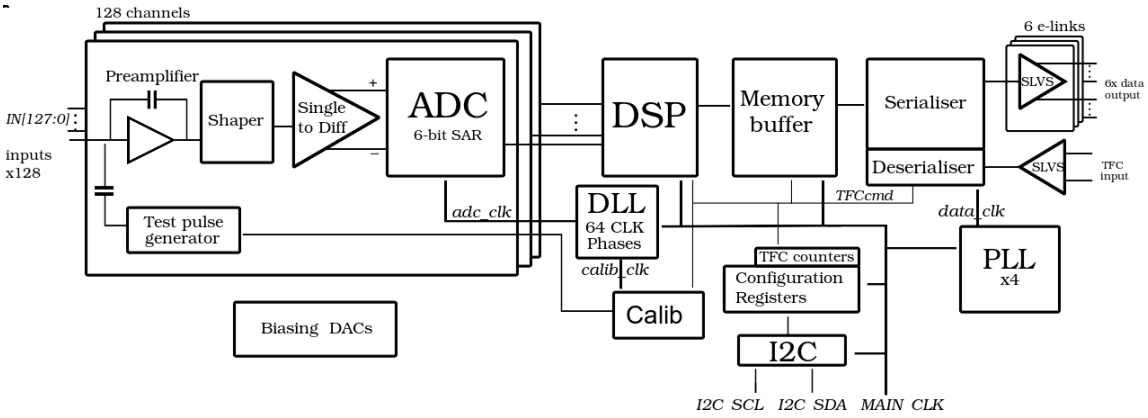
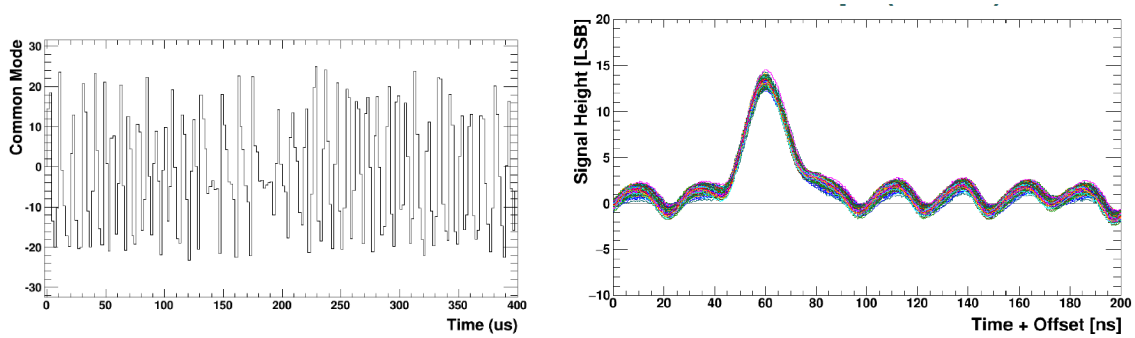


Figure 5: Block diagram of the SALT ASIC signal processing.



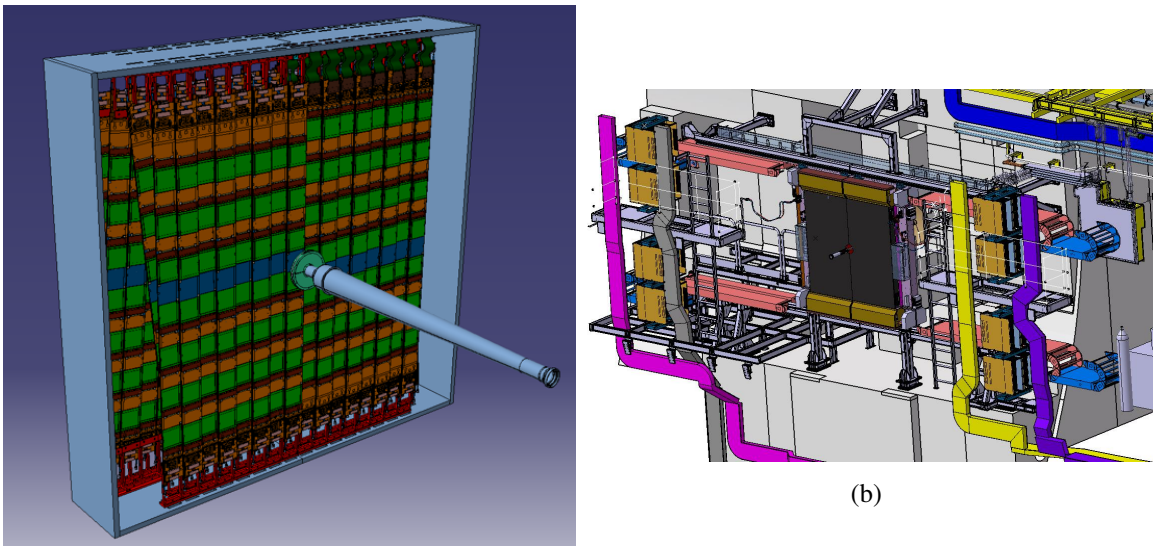
(a) SALT v2 common mode

(b) SALT v3 pulse shape

Figure 6: The SALT v3 revision fixed a major problem with baseline oscillation when simultaneously using multiple ASICs connected to a single sensor module. In v2 (a), this oscillation lead to large fluctuations in the common mode. In v3 (b), this problem is now corrected, allowing a good reconstruction of the pulse shape. The 40 MHz ripple visible at other times is a fixed pattern and does not represent noise at the sampling time.

from carbon fiber faces sandwiching a foam interior containing a titanium cooling pipe for CO_2 evaporative cooling. The modules are mounted on both sides of the stave to ensure complete overlap of the active silicon areas. The detector box together with the full mechanics and services in the experimental cavern is illustrated in fig. 7b.

Power, control, and readout signals are routed to and from the modules using three layer flexible printed circuit board cables attached to the stave faces as shown in fig. 8a. At each end of each stave face, the flex cable is connected to a "pigtail" cable as shown in fig. 8b which routes the signals outside the mounting box. The pigtail is made of three flex cables stacked together, each with three metal layers. At each end the cables are joined. These pigtails connect to the periphery electronics processing interface (PEPI), which is housed just above and below the detector in the brown boxes seen in fig. 7b. Inside the PEPI, Data Concentrator Boards (DCBs) hold the GBT chips which transmit the data over fiber to the data acquisition system. The PEPI also routes the



(a) (b)

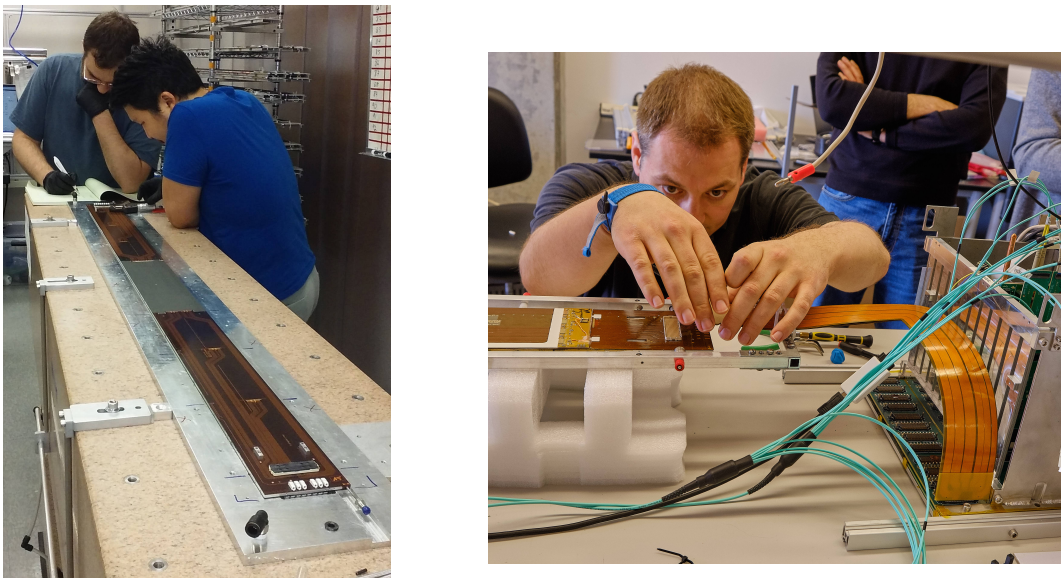
Figure 7: (a) Drawing of the staves mounted inside the UT box. (b) The UT box mounted in the experimental cavern with its full services.

power, control, and monitoring connections for the SALTs and hybrids. The low voltage power is provided by a system of low voltage regulators located in crates visible to the left and right of the detector box seen in fig. 7b

3. UT system tests

The combined sensor and SALT modules have been validated at a beam test conducted at Fermilab in March 2019 [7]. An unirradiated Type A sensor and a Type B sensor irradiated to a fluence of 6.2×10^{13} 1MeVneutron equivalent/cm^2 (more than twice the expected fluence at end-of-life) were tested using SALT v3 ASICs. The experimental conditions at the test were noisier than expected, but the SALT common mode noise subtraction successfully reduced the effect to be equivalent to that obtained with bench tests as shown in fig. 9. The Type A module showed an acceptable signal to noise ratio of approximately 11; the Type B module showed a signal loss from irradiation of about 9%. Scans of the signal peak and the resulting detection efficiency are shown in fig. 10. Because of the data acquisition system used, a high zero suppression threshold was required in the test, resulting in a loss of some efficiency especially for the irradiated sensor. This limitation will not be present in the final system; extrapolating to the expected threshold we anticipate an efficiency better than 99.5%. This leads to an expected efficiency to detect a charged particle in three out of four planes of about 99.99%.

The integrated readout and control systems were also tested during 2019. One stave was instrumented with a full complement of hybrid circuits with SALT ASICs; one production sensor was mounted in the most central position. The stave was mounted and connected to the cooling and readout electronics. When operating all SALT ASICs simultaneously, results were obtained



(a) Stave with flex

(b) Flex–pigtail connection

Figure 8: Power, control, and data signals are routed from the modules by (a) flex cables attached to the stave faces that are connected to (b) pigtail cables which carry the connections outside the UT box.

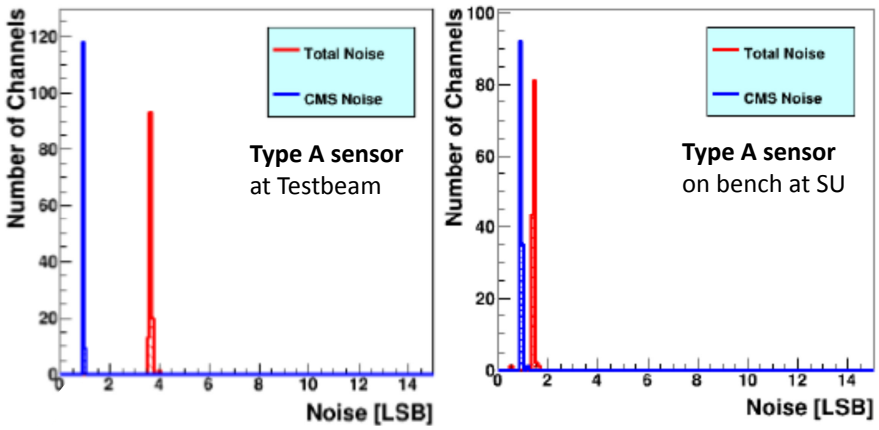
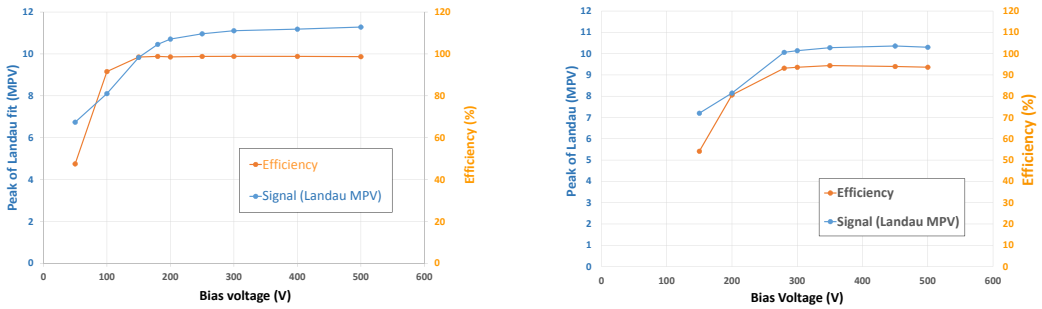


Figure 9: Noise before and after SALT common-mode subtraction (CMS), comparing the result at the beam test with that obtained from bench tests in the lab at Syracuse University (SU). From Ref. [7].



(a) Unirradiated type A

(b) Irradiated type B

Figure 10: Signal pulse height and detection efficiency as a function of applied bias voltage from the beam test of an unirradiated Type A sensor, and a type B sensor irradiated to twice the expected maximum fluence. From Ref. [7].

showing test-pulse shape and noise results consistent with the expectations from single module tests as shown in fig. 11.

This test setup has also produced valuable installation and operational experience. The stave mounting and connection procedure has been refined. Operation of the cooling system is being tested. It also allows for the development of the readout and detector control firmware and software in a realistic setup. These experiences will form the basis for the installation and commissioning of the full detector in 2020.

4. Outlook and conclusions

All components for UT construction are currently produced or in production. Final assembly and installation of the fully instrumented staves will be ongoing throughout 2020. The beam test performed in 2019 has demonstrated that the performance of the final UT modules meets the detector requirements. Integrated system tests with populated staves have provided essential experience for the installation and commissioning of the full detector.

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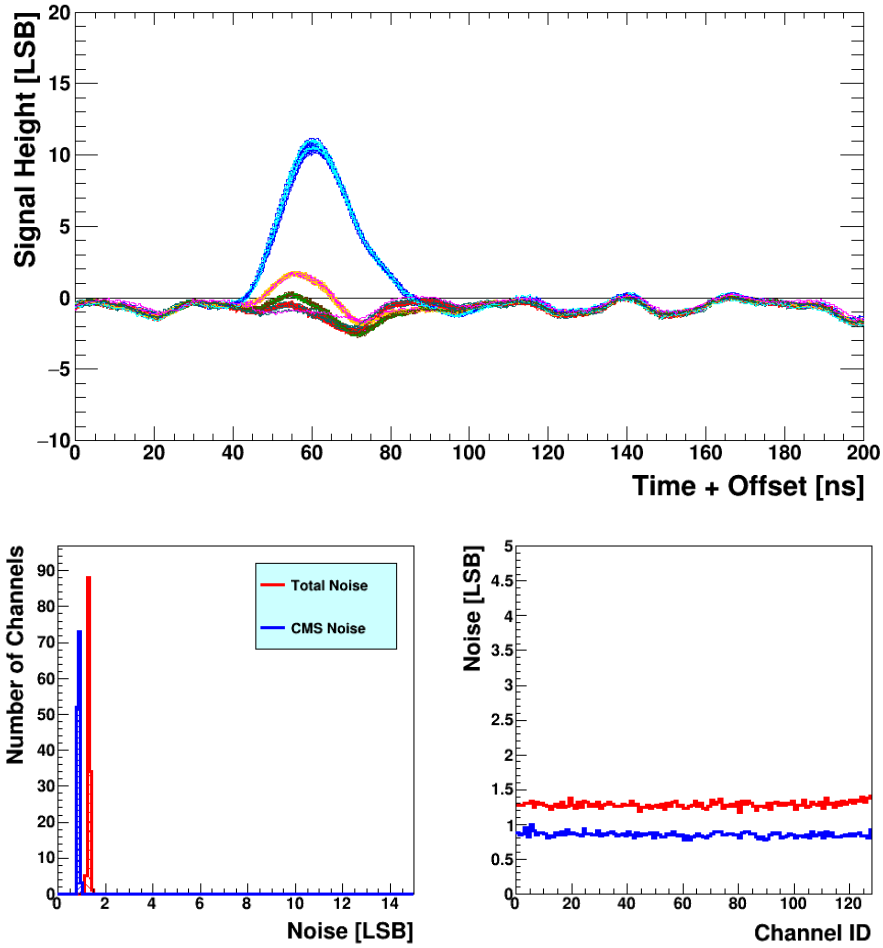

Figure 11: Test pulse shape and noise levels for a single SALT ASIC when operating the full test stave (top) the reconstructed pulse shape obtained in the manner described for fig. 6b where different colors represent different channels and only some of them have injected charge, and (bottom) the total and common-mode subtracted noise levels for each SALT channel both histogrammed over all channels and as a function of the channel ID.

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