Status and Perspectives of an ILC Vertex Detector

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The physics case of the International Linear Collider (ILC) is intended to encompass detailed studies of the Higgs boson and top-quark sectors as well as of fermion-pair production, complemented with direct searches for BSM physics manifestations. All these components of the physics programme involve flavour specific dynamical content, which calls for unprecedented performances of the charged particle detectors composing the experiments, special attention being devoted to the possibility to achieve high performance flavour tagging. The latter relies on a spatial resolution per detector layer of a few micrometres in both directions, combined with a material budget not exceeding 0.15 % of radiation length. This challenging objective is pursued by taking advantage of the moderate radiation tolerance and read-out speed required, combined with the possibility to exploit the machine duty cycle for power saving.

Since the delivery of the ILC TDR in 2012/13, substantial progress was achieved to develop a vertex detector fully suited to the physics requirements. Several pixel sensor approaches were followed, both from the sensing technology and the read-out architecture points of view. They are motivated by the capability to suppress the impact of beam related background, which dominates the hit density of the vertex detector, and tends to grow as the nominal luminosity of the ILC is being extended to 4 to 6 times the baseline values. The paper summarises the performances achieved as well as the status and the perspectives of the different approaches. It shows that the possibility opens up to realise single bunch tagging with square pixels featuring less than 20 μm pitch and associated to a power consumption compatible with air cooling.

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1. Introduction

An electron-positron collider authorising high precision studies of the Higgs boson and top quark characteristics, while simultaneously opening the door to manifestations of BSM physics unlikely to be observed at LHC, is a project driving detector R&D activities since more than two decades. The relevance of its physics programme depends crucially on the achievable detector performances in terms of flavour tagging and charged particle tracking. A vertex detector suited to such a collider intervenes notably in both of these aspects.

The International Linear Collider (ILC) is the most advanced of the different options considered for such a future e^+e^- machine. The development of its concept, based on supra-conductive accelerating units operated at 1.3 GHz, is carried on since the late nineties and has reached a degree of maturity allowing to envisage its construction. The ILC features also the most convenient running conditions as far as vertex detectors are concerned.

A long term R&D is on-going to realise a vertex detector design optimally suited to the ILC physics programme, taking full advantage of the machine assets and of the progress made by industry. The design of the detector differs from most other vertex detectors by privileging physics oriented requirements (spatial resolution, material budget), exploiting the relatively mild running conditions which allow to compromise the read-out speed and radiation tolerance. Beam related background remains however the main source of performance limitation as it dominates the hit density. It motivates the search for a time resolution allowing for a single bunch tagging.

In the following, some aspects of the ILC machine impacting the vertex detector design are overviewed, followed by an introduction to the vertex detector designs and main features. The status of the R&D on the different pixel technologies considered is summarised next, followed by an outlook exploiting the industrial evolution. At last, the paper is summarised.

2. The International Linear Collider (ILC)

ILC is an e^+e^- collider expected to be hosted in Japan. Its design results from extensive studies performed by a worldwide community of experts. It is described in a Technical Design Report (TDR [1]) published in 2013. The industrialisation of the machine key elements was assessed with the construction of the European XFEL light source [2] and its extensions in the U.S. [3] and Asia.

The machine is intended to provide tuneable center-of-mass energies ranging from 250 GeV to $\gtrsim$ 500 GeV and to be upgradable to $\gtrsim$ 1 TeV. It can also run at energies encompassing the Z-pole. Being linear, the accelerator delivers polarised beams (typically 80 %, resp. 30 %, longitudinal polarisation for electrons, resp. positrons).

Originally optimised for running at 500 GeV, the present design concentrates on 250 GeV. The physics programme is supposed to start with an instantaneous luminosity L = $1.35 \cdot 10^{34}$ cm^{-2}s^{-1} for an overall power consumption of $\sim$ 130 MW. The possibility to increase the luminosity was studied, indicating that luminosities 4 to 6 times higher [4] than the aforementioned starting value are reachable by increasing the number of bunch trains and crossings (BX) as well as the power consumption (< 300 MW). These values are compared in figure 1 to the luminosities announced in the Conceptual Design Reports of alternative future e^+e^- colliders [5].
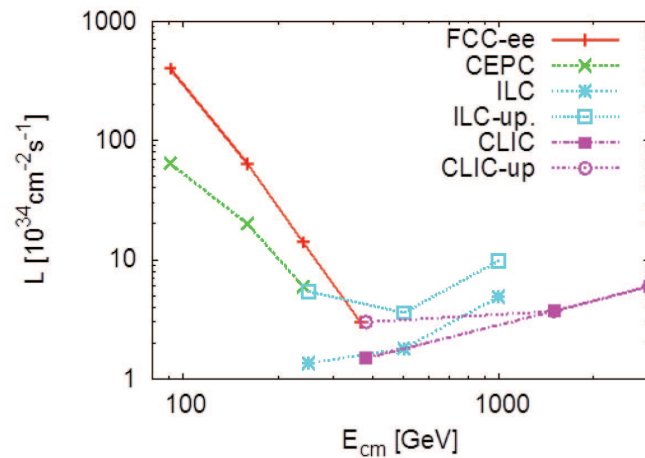
Figure 1: Instantaneous luminosity (L) of the ILC as a function of the center-of-mass energy (E_{cm}), compared to those announced for other e^+e^- machines (CLIC, FCCee, CEPC). The label ILC-up corresponds to a factor four upgrade of the initial value of L.

Present vertex detector requirements at the ILC may account for these highest luminosity expectations as they dictate the beam related background which will dominate the hit density. Another prominent beam parameter is its time structure. The bunch-crossings, separated by a few 100 ns, occur within $\lesssim$ 1 ms long trains separated by nearly 200 ms long beamless periods. This duty cycle allows suppressing the average power consumption of the detector in order to minimise the cooling system needed within the detector fiducial volume. Moreover, the interbunch spacing being relatively long, a time resolution of a few 100 ns is sufficient to separate bunch-crossings.

3. Main Aspects of a Vertex Detector

Two multipurpose experiments (called SiD and ILD) are envisaged to be operated in push-pull mode at the ILC unique interaction point [6]. The vertex detectors of both concepts are optimised for a highly precise reconstruction of the displaced vertices (possibly with their electric charge), including those occurring inside jets. Moreover, the vertex detector is essential for reconstructing soft tracks which, due to the high solenoidal field of the experiments (3.5 - 5 T), deliver little information in the other tracking systems because of their distance to the IP.

The reconstruction of displaced vertices is achieved with very granular pixel sensors delivering a single point resolution of about 3 μm in both directions, and composing detector layers featuring overall $\lesssim$ 0.15 % X_0. The ambitioned spatial resolution may be illustrated with the two-dimensional precision on the distance of closest approach (DCA), parametrised in a usual way, where the standard deviation $\sigma_{r\phi,Z}$ on the reconstructed DCA amounts to:

$\sigma_{r\phi,Z} \leq 5 \oplus 10/p \cdot sin^{3/2}\theta \ \mu m$,

where p, resp. θ, stand for the particle momentum, resp. production angle w.r.t. the beam axis. The corresponding degree of performance may be illustrated by replacing each detector layer with

the ATLAS-IBL pixels and material budget [7], which results in the following parametrisation of the DCA in the plane perpendicular to the beam axis, where the pixels are most accurate:

$\sigma_{r\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta \ \mu m.$

The comparison is displayed in figure 2; it shows the substantial improvement anticipated from the ILC vertex detector concept.
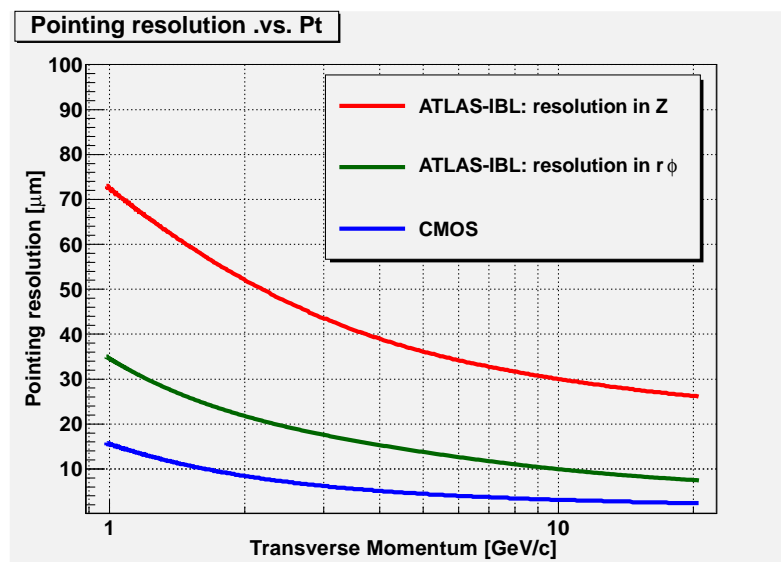
Figure 2: The blue curve displays the transverse momentum dependence of the pointing resolution for an ILC vertex detector in both dimensions, based on 3 μm resolution in both directions and on 0.15 % X_0 per detector layer. The red and green curves display the resolution expected by replacing each layer with an ATLAS-IBL equivalent layer. The latter features 50 x 250 μm^2 pixels and 1 % X_0 material budget.

The realism of this performance, based on intensive R&D pursued since about two decades, underlies the next sections. Two alternative vertex detector geometries, are considered: SiD features a short cylindrical barrel made of 5 equally spaced single layers, complemented with disks in each end-cap. ILD instead, relies on a long barrel composed of 3 equally spaced double-sided layers. Both designs encompass radii ranging from 14 or 16 mm to 60 mm. Several pixel technologies are considered, which are described in the next section.

The constraints coming from the running conditions are dominated by the hits due to beamstrahlung e$^{\pm}$ generated during the crossing of the particle bunches. Some of them are generated at the IP, some others originate from beam elements or end-cap detectors hit by beamstrahlung photons about 3.5 m away from the IP. Because of their low momentum, the core of the beamstrahlung e$^{\pm}$ remains confined inside the beam pipe by the high solenoidal field of the experiments. This core expands on both sides of the IP and determines the limit of the detector geometrical acceptance at shallow polar angles.

The rate of this background, essentially proportional to the luminosity, governs the time resolution requirements of the detector and tends to dominate the required radiation tolerance. The latter amounts to an integraded ionising dose of O(100) kRad/yr and to a non-ionising dose $< 10^{12}$ n$_{eq}$/cm^2/yr.

The Monte-Carlo simulation of the beamstrahlung related hit rate suffers from uncertainties accounted for with safety factors of at least 3-5. The sensors may therefore need to comply with up

to several tens of hits/cm^2/BX [8]. In order to minimise the disturbance generated by beamstrahlung e$^\pm$ overlapping a final state of interest, the detector read-out may be pushed to single bunch tagging or nearly so, i.e. $\lesssim 1$ μs time resolution. This goal has however to comply with the governing constraint of suppressed material budget, which imposes keeping the average power density to modest values (typically $\lesssim 20$ mW/cm^2) compatible with air flow cooling. This constraint may not apply as strictly to the innermost detector layer because of its modest surface (~ 10 % of the total detector surface). Moreover, it may be alleviated if micro-channel cooling can be implemented.

As will be shown in the next section, two alternative read-out options are considered to address this issue: one approach is based on a swift and continuous read-out during the bunch trains, followed by minimal activity inbetween consecutive trains to save power. Alternatively, the hit pixel information may be stored inside the pixel array during the train, the read-out occurring only inbetween consecutive trains at reduced pace.

4. On-going R&D on Pixel Technologies and System Integration Aspects

Most of the R&D effort for an ILC vertex detector concentrated on developing novel pixel sensors, which would achieve a spatial resolution and a material budget well beyond the LHC standard. Various alternative pixel technologies were developed during up to 2 decades, several of them having reached already quite satisfactory results at the time of the TDR (2012) [6].

These results were obtained by compromising somewhat the read-out time. Improving the latter drove most of the sensor R&D in recent years. The associated challenge follows from the very small size of the pixels imposed by the ambitioned spatial resolution and from the very limited power consumption compatible with the allowed material budget.

Some aspects of the different technologies developed are provided in the next subsections. The latter concentrate on specific aspects of each technology, its most recent progress and on its expected evolution in the coming 5-10 years.

4.1 Fine Pixel CCD

Fine Pixel Charge Coupled Devices (FPCCD) are highly granular CCDs featuring 5 x 5 μm^2 pixels, where the signal charge is stored during the full train, and transferred through the sensor bulk at the end of the train to the read-out electronics located at the ladder end. The charge-to-signal conversion and signal transfer are performed at minimal speed, exploiting the beamless period between consecutive trains, in order to minimise the power consumption.

With a single point resolution of $\simeq 1$ μm, it is the most precise of all sensor options considered. It features very low power consumption inside the fiducial volume. Moreover, industry is expected to produce 50 μm thin sensor slabs with full ladder dimensions, which minimises the material budget of the mechanical support. To suppress the bulk damage generated by impinging particles, the detector should be operated within gaseous nitrogen cooled at -90$°$C.

The high spatial resolution allows to recognise a significant fraction of hit patterns coming from beamstrahlung e$^\pm$, which can easily be discarded from the event reconstruction. This approach requires special attention to the power needed to read out the large assembly of pixels and is exposed to the danger of a high hit occupancy complicating the event reconstruction, thereby possibly degrading its quality.

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At present, the R&D addresses the tests of full scale, 120 x 15 mm^2 large and 50 μm thin prototypes featuring 5x5 μm^2 pixels, the development of the charge encoding ADCs and the prototyping of a nitrogen-based cooling system required to achieve the necessary radiation tolerance (see for instance [9]).

4.2 DEPFET

DEPFET Pixel Sensors (DPS) allow for very light structures where the pixel array and the mechanical support are unified in the same piece of silicon. The signal charge is sensed directly in each pixel and the resulting electronic signal is clocked out of the pixel array on a row-by-row basis with very low power consumption inside the fiducial volume, the signal processing chain being located at the ladder end. It includes an ADC which allows exploiting the charge sharing inside a cluster to achieve the targeted spatial resolution.

The sensors are read out continuously during the trains, at a speed reflecting the number of rows composing a sensor, combined with the clock frequency. The necessary spatial resolution is anticipated to be achievable with 20 x 20 μm^2 pixels read out every 25 μs.

The first use of DPS in a particle physics experiment occurred in the recently commissioned BELLE-2 experiment at KEK. They equip the two single-sided layers of the vertex detector (PXD), corresponding each to 0.19 % X_0. The required spatial resolution and sensor thickness is relaxed w.r.t. ILC, allowing for a 20 μs read-out time [10]. Extending the concept to the ILC requires reoptimising the trade-off between pixel dimensions, sensor thickness and read-out time.

4.3 SoI

The technology of Silicon on Insulator (SoI) is widely used for X-Ray detection but was never implemented in a subatomic physics experiment. Its development for the latter domain is still in a rather early stage but provided already promising results. As compared to other technologies, in particular to CPS (see next sub-section), its assets rely mainly on the high density in-pixel circuitry offered, particularly with the double-tier option recently addressed. The latter allows to stack and interconnect two chips on top of each other at the pixel level. Consequently, more functionalities may be integrated in each pixel. Alternatively, the pixel size may be squeezed to comply with the ambitioned spatial resolution of $\lesssim 3$ μm.

The on-going prototyping is based on a delayed read-out architecture, where each 20 x 20 μm^2 pixel hosts multi-hit signal and timing memories delivering a timestamp of the hits detected. The position and timing informations of the full ILC train are stored in the pixel array and read out inbetween the trains. A prominent result of the prototyping is the validation of the pixel-to-pixel interconnection technique based on 3.5 μm large micro-bumps [11].

4.4 CMOS Pixel Sensors (CPS)

CPS are being developed since two decades for an ILC vertex detector and have thereby introduced the technology in subatomic physics experiments. The first vertex detector using CPS was the STAR-HFT which was operated successfully from 2014 to 2016 at RHIC/BNL [12]. Its 50 μm thin sensors, manufactured in a 0.35 μm CMOS process, provided a single point resolution better than 4 μm and a time resolution < 200 μs based on a rolling shutter read-out.

A more powerful CMOS technology with a 0.18 μm feature size was used more recently to realise the CPS ALPIDE equipping the $\sim 10\ m^2$ large ALICE-ITS2 tracking sub-system being assembled at CERN in perspective of the LHC run starting in 2021. This CMOS process allowed to integrate a shaping and discriminating circuitry inside each pixel, combined with a sparse data scan logic, which results into a substantial higher hit rate capability and a reduced power consumption. The pixel size had however to be enlarged, translating into a spatial resolution of $\sim 5\ \mu m$, for the benefit of a data driven continuous read-out architecture featuring a 10 μs read-out time.

The same process is presently used to develop the MIMOSIS sensor for the vertex detector (MVD) of the CBM experiment at FAIR/GSI. Its design extends the ALPIDE architecture to comply with more severe running conditions (e.g. 50 times higher hit rate and data throughput as well as a twice faster read-out). After three years of R&D, the first full scale prototype, composed of 0.5 million 28x30 μm^2 pixels with 5 μs read-out time, is being fabricated. Its design is a possible baseline for the PSIRA sensor envisaged for an ILC vertex detector. An earlier prototype of MIMOSIS, composed of only part of the pixel array (64 columns of 504 pixels) and digital signal processing circuitry, has shown that the front-end allows for a read-out below 1 μs [13], which indicates that single-bunch tagging, based on a O(500 ns) read-out time, may be reached. However, substantial R&D is still demanded to shrink the pixel size to match a 3 μm spatial resolution.

An alternative approach based on CPS is pursued within the Chronopixel project [14]. The design singularity is that it gives priority to time stamping each hit with a few hundred nanoseconds precision, thereby associating the latter to the bunch crossing which has generated it. The time stamp may be memorised inside the pixels, which would be read out inbetween consecutive trains. The prototyping has gone through 3 prototyping steps, based on 180 and 90 nm triple-well CMOS technologies. The time stamping was prototyped with pixels containing two 14-bit memory cells to record the time stamp and a calibration circuit to compensate for comparator offsets. Other prototypes addressed the optimisation of the sensing diode parametres. An important future step will consist in realising a complete sensor featuring pixels small enough to comply with the required spatial resolution while hosting a circuitry capable of single bunch tagging.

4.5 Other options

As shown above, none of the R&D pursued up to now demonstrated that a spatial resolution of $\lesssim 3\ \mu m$ and a single bunch stamping are achievable simultaneously within the same sensor, moreover with a power consumption compatible with air cooling. Two types of alternative approaches are therefore being considered. They either provide the ambitioned spatial and time resolutions, respectively $\lesssim 3\ \mu m$ and $\lesssim 500$ ns, in separate sensors, or derive the spatial resolution from the combination of two independent measurements of the impact position delivered by sensors providing the ambitioned time resolution.

One approach consists in equipping one of the detector layers with fast sensors, less granular than those of the other layers, which provide the necessary spatial resolution. The track reconstruction will associate a hit generated in the time stamping layer to the corresponding hits generated in the high resolution layers, thereby assigning to each reconstructed particle trajectory the required spatial and temporal resolutions. The technology of the fast sensors may be CMOS or LGAD.

Another approach anticipates that an extension of MIMOSIS could provide a time stamp of a few hundred nanoseconds resolution with pixels small enough to deliver $\sim 4\ \mu m$ spatial resolution.

By combining the positions of the two impacts generated by particles traversing a double-sided layer, one obtains the position of the hit with a resolution amounting to $\sim 70\ \%$ of a single pixel resolution, thereby reaching the ambitioned $\lesssim 3\ \mu m$.

5. Outlook

Sizeable performance improvement is awaited in the coming years from industrial progress. An emblematic example comes from ASIC production, which drives steady miniaturisation of integrated circuits. CMOS foundries also offer the possibility of stitching, which allows for wafer-scale sensors. Once thinned to a few tens of microns, the sensor may be curved according to a cylindrical surface, with a sizeable gain in stiffness. A few sensors only are then required to equip a complete detector layer, with a drastic suppression of mechanical support material consecutive to the disappearance of overlaps between neighbouring detector modules. This concept is promoted by the ALICE collaboration, which aims for an upgrade of its vertex detector [15]. Maximum benefit is expected for the innermost detector layer, where the beam pipe may act as a mechanical support.

Stitching is available in the TJsc 180 nm process used for ALPIDE and MIMOSIS. It is also accessible in a forthcoming 65 nm imaging process investigated for the purpose of the ALICE upgrade, within a partnership involving groups interested in various applications, including ILC related tracking devices. The process should in particular allow for reduced pixel dimensions, and therefore improved single point resolution. Overall, the evolution toward this 65 nm CMOS process is particularly promising and should benefit from a cross-fertilisation between numerous projects.

Another promising R&D direction addresses the realisation of two-tier chips interconnected at the pixel level through industrial micro-bonding techniques. High-density micro-bonding is becoming widespread, which allows to distribute the analog front-end and the digital circuitry of a pixel among two different chips being ultimately interconnected at the pixel level. The result is a reduced pixel size which improves the spatial resolution and enhances the data compression. This approach, pioneered with SoI sensors, is getting extended to CPS.

6. Summary

The ILC project is evolving toward a worldwide preparatory phase which makes it become a concrete opportunity for a Higgs factory. Its physics performance will largely rely on jet flavour identification, calling for a vertex detector featuring a spatial resolution and a material budget never achieved elsewhere. These challenging requirements are addressed with various pixel technologies by compromising the time resolution to a tolerable degree (w.r.t. occupancy by beam related background) and taking advantage of the modest radiation load foreseen.

The performances achieved up to now are quite satisfactory w.r.t. the specifications expressed in the ILC TDR, published in 2012. Improvement is however desirable as far as the tension between granularity and time resolution (versus occupancy) is concerned. Other issues remain also pending, which impact the detector material budget (e.g. power cycling, cooling).

These pending questions get enhanced by the perspective of an increased machine luminosity, which can be envisaged realistically given the maturity of the accelerator design. The consecutive

increase of the beam related background strengthens the motivation for sensors offering a single bunch-tagging capability, i.e. a time resolution of a few 100 ns. On the other hand, the ambitioned spatial resolution calls for a pixel pitch of about 20 μm or less, depending on the charge encoding granularity. Two R&D approaches are followed to match these objectives in a single pixel: a newly available 65 nm CMOS technology and the possibility to realise a double-tier pixel array. Another R&D activity addresses the goal of multi-reticle sensors, which greatly suppress the material budget of the detector layers, in particular for the innermost one. Power consumption comes into consideration with a slightly attenuated importance because of the accelerator duty cycle and inter-bunch spacing, which allows for power cycling the detector and a time resolution with moderate impact on the sensor powering.

Several of these studies are also relevant for heavy-ion physics experiments and should benefit from a substantial overall synergy. It seems therefore likely that within the coming decade, the feasibility of a vertex detector fully complying with the ambitioned performances will emerge.

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