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Prototype Module Construction for the High Luminosity Upgrade of the CMS Pixel Detector

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With the planned upgrades of the LHC towards high luminosity operation, the entire CMS silicon tracker will be replaced in order to cope with the resulting elevated pileup and radiation levels. To fulfill these requirements for the CMS pixel detector, a new readout chip was developed by the RD53 collaboration in 65 nm CMOS technology, featuring a higher readout bandwidth along with increased granularity and radiation tolerance. These chips are operated at high currents rendering the classical parallel powering of individual devices inefficient. A serial powering concept was therefore developed where the input current is shared by a chain of devices. This reduces considerably the power loss in the detector services thus keeping the requirements for powering and cooling at acceptable levels. Based on the availability of the Shunt-LDO, a voltage regulator compatible with the serial powering scheme, on the RD53 chip, a novel module concept was developed. This paper presents the module design and implementation based on the prototype RD53A devices which were evaluated in single operation and as part of a serial powering scheme.

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1. Introduction

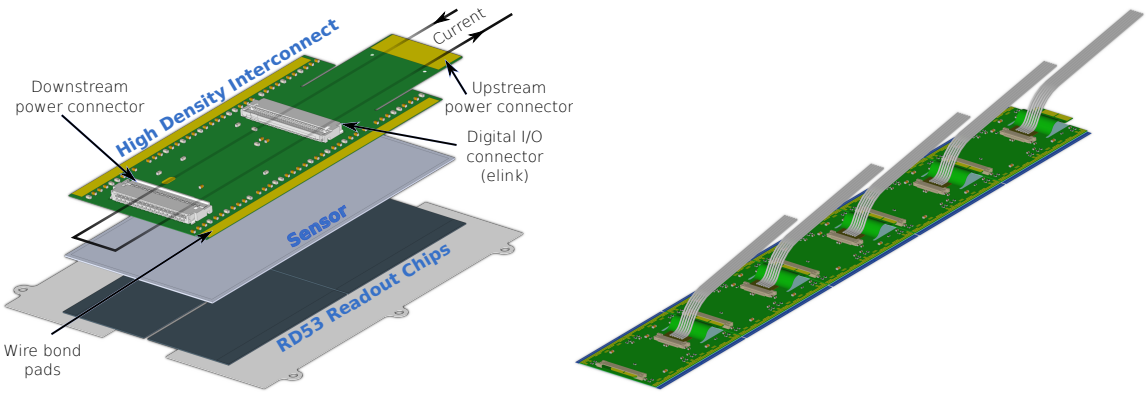
By 2026, the Large Hadron Collider (LHC) at CERN will be upgraded towards high luminosity operation, boosting its instantaneous luminosity to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. This will lead to a significant increase of pileup from the current value of 40 – 60 up to 200 and to unprecedented radiation levels. In such an environment, the current CMS pixel detector [1, 2] would be unable to sustain efficient operation and will be entirely replaced. The current structure consisting of a four layer barrel section called BPIX [3] and groups of three end-cap disks at each extremity called FPIX will be extended by another another five disks. A far forward detector with four additional discs at each end of the pixel detector called EPIX will increase acceptance from a pseudorapidity of $\eta = 2.4$ to approximately 4.0 [4].

An elevated hit occupancy of $3.5\,\mathrm{GHz/cm}^2$ necessitates a new readout chip (ROC), which was developed by the CERN RD53 collaboration in 65 nm CMOS technology [4, 5]. This chip features a higher granularity with a pixel size of $50 \times 50\,\mu\mathrm{m}^2$ and an overhauled readout chain supporting the required storage of hit information over the trigger latency of 12.5 µs [4]. To meet the power requirements while keeping a low material budget, a novel powering scheme was implemented in a module concept which will be discussed in this paper.

2. The CMS Inner Tracker module concept

The main challenges for the Inner Tracker in the HL-LHC era will be to cope with the increased pileup and radiation levels while keeping a low material budget. While the pileup is addressed by the RD53 chip mainly by a higher granularity, this comes at a price of increased power consumption. The overall consumption of the Inner Tracker is approximately 50 kW leading to stronger requirements on the cooling [4]. Furthermore, the readout chip is built in a CMOS process with a smaller feature size compared to the current detector. This allows only low supply voltages, hence requires high input currents. To keep voltage drops low over the 100 m long supply lines, the traditional powering scheme of supplying several modules in parallel would lead to an unacceptable increase of cable mass. Instead the modules will be powered in serial chains, where the readout chips are sharing a constant input current and generate the necessary operational voltage themselves. The current that the cabling has to provide is hereby lowered from $N \cdot I_{module}$, with N as the number of modules, to the consumption of one module which decreases the power loss in the cables by N^2 over parallel powering [4].

In order for this scheme to work, the current consumption of each module has to remain constant, independent from the actual load, thus the module has to act as a constant resistor in the chain. This is facilitated by the so called Shunt Low Dropout Regulator (Shunt-LDO) [6], which consists of two parts: A voltage regulator, generating the necessary supply voltages on the chip and in parallel a shunt circuit, which consumes the current, not used by the LDO. The shunt ensures hereby a constant current consumption of the module. Two Shunt-LDOs, powering the analogue and digital domain separately, are implemented in the RD53 design, allowing the devices to be used in this scheme without further active electronics. To mitigate the risk of one failing device breaking the chain, a hybrid approach is envisaged. Here multi-readout chip modules are forming the links in the chain, while the chips themselves are powered in parallel on the module. The current of a



(a) (b)

Figure 1: A 3D rendering of (a) the components of a single module and (b) a serially powered chain of modules as envisaged for the upgraded detector.

failing chip, which would break the chain, is then consumed by the shunt circuits of the other ROCs on the module. In the CMS Inner Tracker chains of up to ten modules will be used with two or four readout chips forming one module. This paper will focus on the modules for the barrel part of the detector. The implementation of such a module and the serial chain is depicted in Figures 1a and b. It consists of a pixelated sensor in Planar Pixel or 3D Silicon technology, which is bump-bonded to two or four RD53 readout chips. Powering and readout signals are routed via the High Density Interconnect (HDI), a flex PCB glued to the sensor and wirebonded to the chips [7]. The powering current enters the module via the pigtail, is distributed in parallel to the readout chips and then exits to the next module via the rear-end FCP connector. The second FCP connector carries the differential lines for control and data readout.

A feature of the CMS Inner Tracker is that it can be extracted from the detector for maintenance and repairs. For this, it is divided in two cylinders, connected at the centre of the detector ($z = 0$), with each cylinder further divided into two half-shells. Due to space restrictions, chains of modules cannot be connected at the centre of the detector, hence the current of a half ladder in the barrel section has to return through the same modules to the end of the barrel. The HDIs therefore have to carry twice the supply current with minimal losses as not to add to the thermal budget of the detector and also not to heat up the sensor, which is crucial after irradiation. A PCB consisting of three copper layers, supported by polyimide foils is prototyped in view of these requirements. While the input current is routed to the ROCs on the top plane, the bottom plane carries the output current of the ROCs to the rear connector. The internal plane is dedicated to conducting the return current between the connectors. Power simulations showed that this design ensures a power loss over the HDI at nominal current of 5 A for four chip modules of less than 200 mW per layer [7]. This will be further decreased in a revised design, currently in production.

The material budget of the module was calculated using the layer stack information, provided by the manufacturer and the material composition and thickness of the loaded components. The volume of each component type was estimated and an average thickness calculated as the relevant thickness. The material budget of the current design for a 2×2 ROCs module was found to be 6.37 ‰, which is in line with what was expected from similar modules built for ATLAS IBL [8].

Component	Material	Avg. thickness [µm]	X_0 [cm]	X/X_0 [‰]
Read-out chip	Silicon	150	9.36	1.60
Sensor	Silicon	150	9.36	1.60
Bump bonding	Tin	2.35	1.21	0.20
HDI	Copper	30	1.44	2.09
	SMT devices	4.0	4.29	0.32
	Polyimide	49	28.58	0.26
	Epoxy glue	75	42.60	0.18
Glue interfaces	Epoxy glue	50	42.60	0.12
Sum				6.37

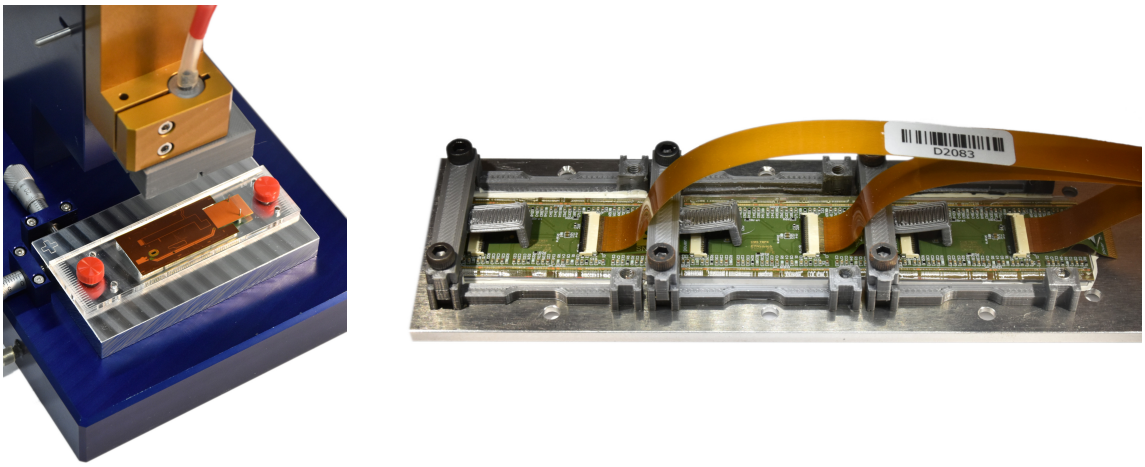
Table 1: Material budget of the barrel pixel 2×2 module in the current design.

If the contributions from the sensor and readout chips are excluded, this is dominated by the copper traces as shown in Table 1. These layers were minimised to a thickness of 10 µm which was found to be an amount necessary to conduct the supply current for four-chip modules without excessive power dissipation. Measurements of the exact material budget via x-ray absorption are in preparation.

3. Prototype module construction for the Inner Tracker

In the effort of developing a readout chip for the HL-LHC pixel detectors of the ATLAS [9] and CMS [10] experiments, the RD53 collaboration designed a prototype chip called RD53A [5]. This device contains three pixel matrices with different analogue signal processing chains or front-ends for evaluation by the tracker communities. Although being half the size of the final chip, it provides a readout and powering scheme close to the final design so it was used to develop and verify the new module concepts. For this, a half-sized HDI was designed with the same features as for the final modules, described in the last section.

A construction procedure was established and so far applied successfully to over 20 modules. It has to be noted, that at that time, no sensors for the RD53A chip were available, therefore so called *digital modules* without actual sensors were built, which suffices for testing the module design and assembly procedures. During construction, readout chips and the HDI are positioned in already available high precision lifts and aligned with the help of cylindrical pins. A 100 µm thick UHU plus endfest 300 epoxy glue layer connects the HDI to the ROCs, which are carried and attached by a vacuum chuck. Great care is taken to ensure that the whole area below the wire bond pads is covered by glue to enable reliable wire bonding to the flex PCB. After curing, this presents the last manufacturing step before testing. The development of the assembly procedure was facilitated by a combination of high precision mechanics like the aforementioned lifts, few alignment chucks and tools using rapid prototyping techniques. The tools for glue application, the vacuum chuck and holding structure for the HDI were refined via FDM 3D printing and laser cutting of acrylic glass sheets. Figure 2a shows the HDI in the lift, holding the ROCs via the vacuum chuck . First prototypes used a silicon slab as dummy sensor for carrying the HDI and the



(a) (b)

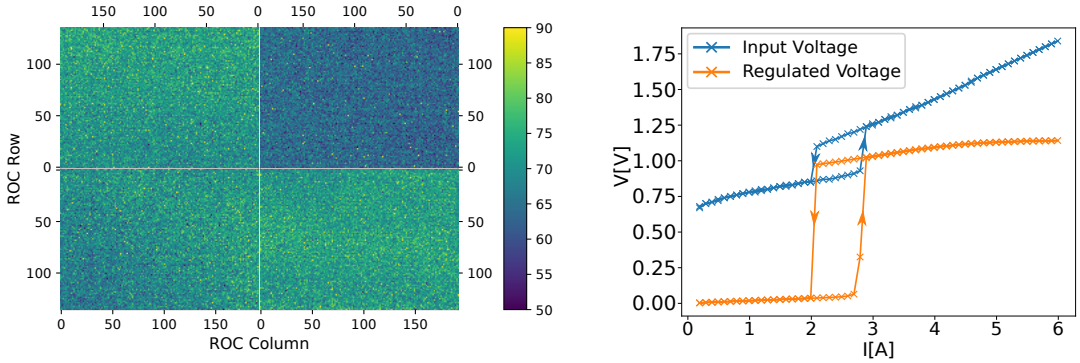
Figure 2: (a) Tooling for the assembly of (digital) modules. The HDI is precisely positioned under the four read out chips, ready for the gluing procedure. (b) A serially powered chain of digital modules.

ROCs, but subsequent trials showed that the HDI itself is stiff enough to support the chips without the slab, simplifying the production.

The modules were characterised via lab measurements with respect to their powering behaviour, communication stability, minimum achievable threshold and electronic noise charge (ENC). Special care was taken for the last point as all chips now share the same ground and communication input. In the per-pixel analogue circuitry, the ENC is the main driver of the imperfection of the discriminators activation behaviour, thus the probability for the discriminator to trigger at a defined input charge. As it smears the theoretical step function into a Gaussian error function, the ENC was defined as the difference in input charge needed to raise the discriminator's hit probability from 30 to 70%. Figure 3a shows the distribution of the ENC per pixel over the four ROCs of a quad-chip module. Except for typical chip to chip variations, the noise behaviour shows no prominent structures and remains around 70 e^- as measured on single-chip PCBs [11].

4. Performance of prototype modules in a serial powering chain

For operation in a serial chain, each module has to fulfill the requirements on power generation and impedance, a stable and noise-free voltage generation and a constant current consumption. As for the RD53 chip, the Shunt-LDO circuit has to be externally wired to the power rails of the actual ROC and its behaviour is evaluated for each chip after assembly to a module. Figure 3b shows the voltage drop over the voltage generator thus its input voltage. Furthermore the regulated voltage is plotted with respect to the input current. One can observe a linear trend before the turn-on point around 2.8 A (for four ROCs), which continues after a jump in impedance. This is caused by a late turn-on of the reference voltage generator and thus the LDO itself, which also results in a jump of the LDO output voltage. While to the external power supply the Shunt-LDO appears as a constant resistor, the regulated voltage reaches its set voltage close to the design value of 1.2 V and is kept



(a) (b)

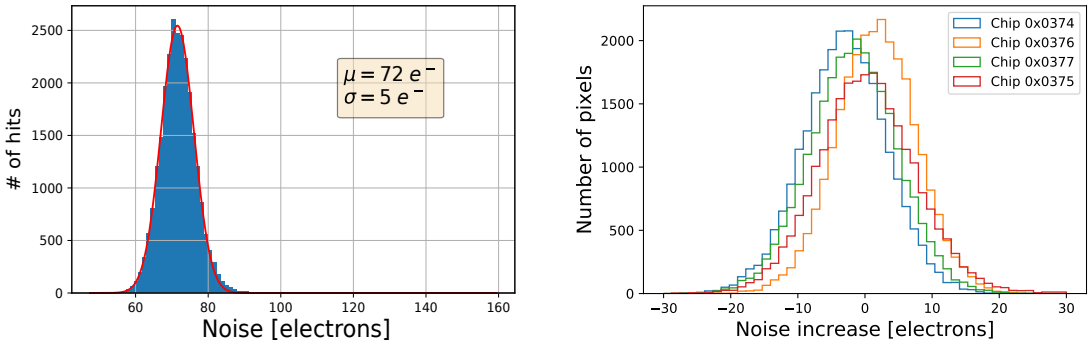
Figure 3: (a) Per pixel ENC map of the four ROCs of a quad-chip module. (b) Input and regulated voltage vs. input current sweeps (ramp-up and down) for a serially powered module.

stable. Although the activation point varies from chip to chip, only one jump at ramp-up is visible, which is a beneficial effect of the current sharing on the module. In a situation when one ROC turns on earlier than the others, it starts consuming less current due to the jump in impedance. The excessive current is then diverted to the remaining chips which then can reach their turn-on point, so all ROCs turn on at the same input current. During operation, the Shunt-LDO can also be powered below the initial activation current, as seen in the ramp-down curve, hence a possible oscillation behaviour close to the turn-on point is prevented.

The Shunt-LDO is required to decouple the regulated voltage from changes on the input side, therefore also the functionality and electronic response to signals should be independent of the operation in a chain. This was verified by measuring the electronic noise charge of the analogue signal chain in the pixel matrix containing the Linear Front-End analogue circuitry [5]. By comparing the ENC of a module in single operation and in the chain, no significant difference was observed. In Figure 4 the noise distribution of the module in single operation and the pixel by pixel difference after inclusion in the serial chain can be seen. All deviations are within the statistical uncertainty of the measurement.

5. Conclusions

A new detector concept based on chains of serially powered two and four chip modules was established for the upgrade of the CMS Inner Tracker detector for HL-LHC operation. First tens of *digital modules* without sensors were built and used in laboratory measurements to verify their functionality in single operation mode and as a serially powered chain of so far three modules. They behave as expected in terms of powering and noise behaviour. With the established assembly procedures, in the order of 100 modules will be built at the production centres as soon as the currently produced sensor-readout-chip assemblies become available. With the recently revised HDI layout this will allow to prove the module concept on a larger scale and in beam based experiments.



(a) (b)

Figure 4: (a) Typical ENC distribution in electrons of an individually powered read out chip and (b) the per-pixel difference after inclusion in a serially powered chain.

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