PROCEEDINGS OF SCIENCE

Low dose rate ^{60}Co facility in Zagreb

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The Co-60 irradiation facility at Ruđer Bošković Institute in Zagreb allows for gamma irradiation in a large range of doses from a maximum of 30kGy/h down to 30Gy/h. Recently, a setup for the radiation tolerance study of readout electronics has been built inside the irradiation chamber. This setup allows for performing tests in conditions similar to ones that will be experienced at HL-LHC experiments. The irradiation dose rate is close to the dose rate at 3cm from the p-p interaction point, the temperature inside cold boxes is controlled by using chilled water and Peltier elements, and the relative humidity is defined by dry air flushed through the cold boxes.

The setup is used for irradiation of ATLAS and CMS pixel detector prototype readout chips, called RD53A. This chip is built in 65 nm CMOS technology that demonstrates a radiation damage dependence on the irradiation dose rate. In this paper the setup itself and a few preliminary results of the radiation damage received at the low dose rate will be presented.

The 28th International Workshop on Vertex Detectors - Vertex2019
13-18 October, 2019
Lopud, Croatia

1. Introduction

Figure 1: Photo of the two cold boxes in the corner of the ^{60}Co facility

The Large Hadron Collider will be upgraded in the coming years so that the instantaneous luminosity increases by a factor of 5-7 with respect to the present one. At the High Luminosity (HL-) LHC, pixel detectors of the two general purpose experiments, ATLAS and CMS, will be placed as close as ~3 cm away from the proton-proton interaction point. During the expected 10 years of operation these detectors will accumulate the total ionisation dose (TID) of about 1-2 Grad. ATLAS and CMS are developing a new readout chip for pixel detectors within the RD53 collaboration. The first prototype of the chip is called RD53A. This chip is realised in 65nm CMOS technology to accommodate the required features.

Radiation tolerance of electronics is usually tested using an extremely high dose rate (HDR) of irradiation to accumulate required TID in a reasonable time period, i.e. an equivalent dose to 10 years of the HL-LHC is collected in a few days. However, recent results [1] show that the radiation damage of 65nm CMOS devices depends on the dose rate, they degrade faster at the lower dose rate (LDR) than at the HDR. This phenomenon, called Enhanced Low Dose-Rate Sensitivity (ELDRS), should be investigated and, ideally, quantified for qualification of RD53A readout chips [2] that will be used in the low irradiation dose rate environment, like at HL-LHC.

A setup that allows for irradiation of the RD53A chips at the low dose rate in a cooled environment and with constant monitoring was built inside an irradiation chamber of the ^{60}Co facility at RBI (*Ruđer Bošković Institute*) in Zagreb.

2. ^{60}Co facility

The ^{60}Co facility in Zagreb hosts a panoramic gamma ^{60}Co source. ^{60}Co is an isotope with a half-life of 5.27 years that emits mainly two photons with energies 1.17 MeV and 1.33 MeV. At these energies, the Compton scattering is the prevalent mode of interaction with matter. The source consists of 24 hollow guiding rods arranged in a cylindrical geometry with a radius of 13

cm. Each rod contains four capsules with a cobalt pencil of 8 cm length. The total activity of the source is around 2 PBq.

The irradiation chamber is separated from the control room with a thick concrete wall. The chamber is accessed through a corridor separated by a 1.5m thick concrete wall. Large samples are placed around the source where the dose rate ranges from 500 krad/h down to 1krad/h of water equivalent dose. The small samples can be placed in the center of the cylinder where the dose rate is about 2.5 Mrad/h.

3. Experimental setup

To investigate the ELDRS phenomenon of the RD53A chip a test setup was built at the RBI ^{60}Co irradiation facility. The goal of the study was to irradiate RD53A chips under conditions close to the operational ones. The following requirements were fulfilled. The dose rate was similar to the one that will be at 3 cm from the proton-proton interaction point at the HL-LHC. ATLAS and CMS pixel detector will be cooled during operation, hence the RD53A chips have been irradiated in a cold and dry atmosphere inside thermally isolated styrofoam boxes (two white boxes in Fig.1). The chips were attached to copper plates with a thermal paste. The plates were cooled by radiation-hard Peltier elements, heat was removed by liquid cooled down by a chiller. Finally, the chips have been powered and connected to the readout system, placed in the control room. That allowed for constant monitoring of operational conditions and parameters, and for testing their functionality and performance at different TIDs.

The test setup was placed in the corner of the irradiation chamber closest to the source. The dose rate in this location, that is 120 cm away from the center of the 60C0 sources, is about 36 krad/h. Necessary cables and pipes were routed through the corridor that connects the irradiation chamber and the control room. Front-end electronics were placed in the corridor, while PCs, power supply units (PSU) and monitoring devices were located in the control room. The chiller and the dry air bottles were located outside the control room.

3.1 Cooling system

Six RD53A chips were divided into two groups of three. The first group of chips was placed in a pilot cold box setup and irradiated at room temperature: first, without an active cooling and, later, cooled only with chilled liquid. The second group of chips was operated in the second cold box at a lower temperature controlled by Peltier elements.

The cooling system consisted of a chiller, dry air supply and cooling plates. Peltier elements were fixed with thermal paste to on of the cooling plates. The chiller pumped coolant through the pipes connected to copper plates. The coolant temperature was set to +15°C. In the pilot cold box, the chips were cooled only by the chiller and, hence, operated at the temperature of about +20°C. In the cold box chips were supposed to be cooled down well below 0°C (e.g. -10°C). Unfortunately, the dry air system was able to provide an air flux maximum of 1.5l/min which was not sufficient to keep the humidity low enough at temperatures below 0°C. Therefore, the minimum achievable temperature was a few degrees Celsius above 0. In addition, due to the not ideal contact between the chips and the copper plate, the real operational temperatures were +5°C, +8°C and +15°C. The Peltiers and the chiller were not controlled and

operated at constant power. Fluctuations of the environmental temperature outside caused variations of the coolant temperature directly affecting the temperature of the chips as can be seen in Fig. 2. The fifth chip is not shown because the connection to it was lost after installation of the cooling system.

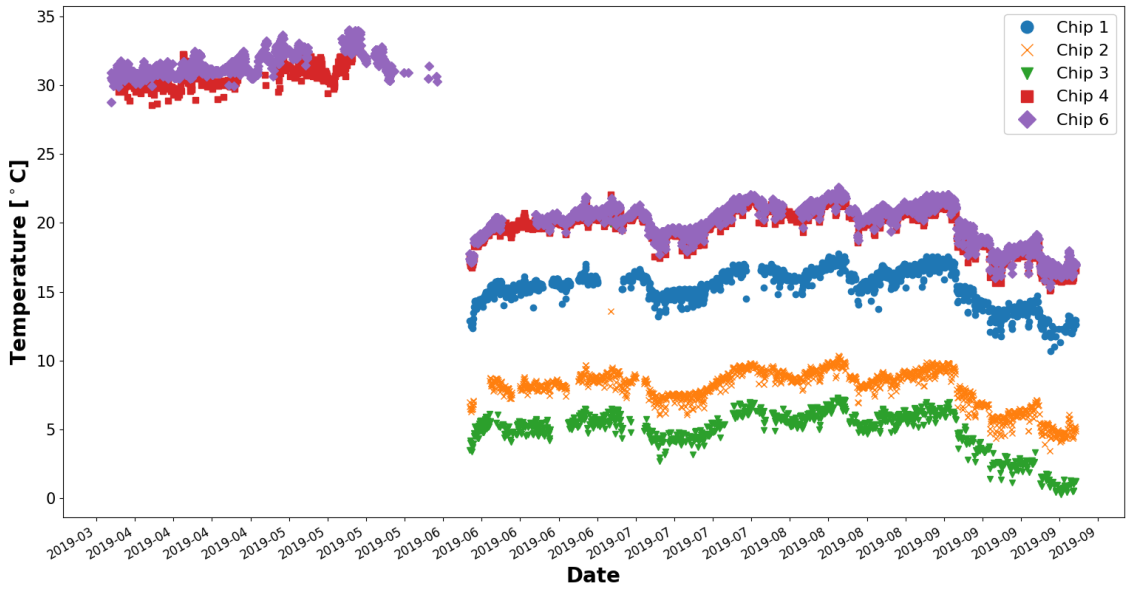

Figure 2: Temperature for chips cooled with Peltiers (1-3) and two chips without Peltier cooling (4 and 6). The Peltier cooled chips were not at the same temperature due to the different qualities in their thermal contact. Chips 4 and 6 were connected before cooling installation which explains the temperature drop in June.

Dry air was supplied from the dry air bottles located just outside the control room. Two dry air bottles were connected to an automatically-switching system which provided dry-air from the second bottle, once the first one was exhausted. This ensured continuous supply between bottle exchanges. There was no humidity monitoring in the cold box. During the installation, a humidity sensor was placed in a cold box to measure humidity and dew point at various dry air flow rates. On the basis of these measurements, it was decided to run the setup at 1.5 l/min. At this flux a single dry-air bottle is spent and substituted every two and a half days. The dew-point for this flux was around +2℃ so the chips were cooled as low as +5℃.

3.2 Readout

Communication with the RD53A chip was done using a commercial, Kintex-7 FPGA, evaluation kit connected to a PC. Each chip had its own data acquisition, a control system, and a PSU. To guarantee the stable communication with the chips, the length of the display port cables, connecting the chips to the FPGAs, was limited to 5m. The FPGA boards were placed behind a 1.5m concrete wall to protect them from radiation. The boards were connected with a 20m ethernet cable to the PCs that together with PSUs were located in the control room.

Custom developed readout software was used to communicate with the RD53A chips. Chips were permanently kept active by injecting internal calibrate signal in every pixel unit cell

of the pixel matrix and driving test structures called ring oscillators[2] (RO). The RD53A chip contains eight RO test structures. They differ in the type of gates, driving strengths and transistor sizes. Frequency of the ROs depend on the TID and provide information on gates time delay. A pixel matrix characterization and RO frequency measurements were performed every hour. Since RD53A chip performance parameters (threshold, noise, etc.) change with TID, all chips have been re-calibrated once a day.

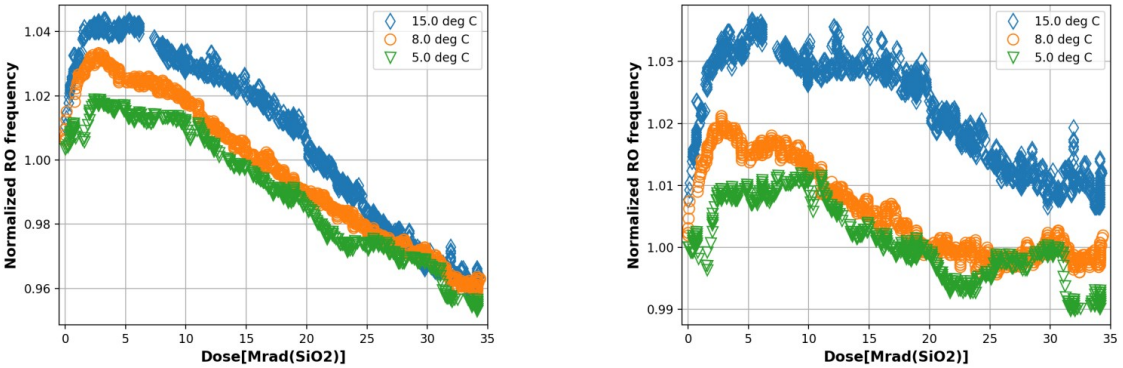

Figure 3: Comparison of the InverterClock ring oscillator structure with driving strength 0 (left) and driving strength 4 (right). Ring oscillator frequency is normalized to unity at the start of irradiation. Fluctuations in the frequency originate from temperature fluctuations. Average chip temperature is in the legend.

3.3 Dosimetry

The dose rate measurements were performed using ethanol-chlorobenzene (ECB) dosimeters (ISO/ASTM 51538:2017). The dosimeters were placed on the front sides of the cold boxes. The dose rates measured in the pilot cold box is 31 krad/h, while in the colder one it is 29 krad/h. The dose rate measured with ECB dosimeters has been verified using the Geant4 simulation [3].

4. Preliminary results

The data analysis is not yet completed so only preliminary results are presented. In Fig. 3, the frequency relative changes of two ROs are shown for three different chips. The frequency of the ROs change as a consequence of the combination of effects induced by irradiation to the

[2]A ring oscillator is a device composed of an odd number of inverter gates in a ring, whose output oscillates between two voltage levels, representing true and false. The inverters, are attached in a chain and the output of the last inverter is fed back into the first. The requirement for odd number of gates ensures that the output of the last gate is the opposite of the input of the first gate. This means that the input to the first gate will oscillate between values of zero and one, giving the name "ring oscillator".

transistors in the digital gates as explained in [1]. A small increase of the frequency is observed at the beginning of the irradiation campaign, induced by an increase of the current that the transistors drive, which is compensated by a following effect that reduces this current and that becomes dominant during the rest of the campaign. This change of behaviour stems from different trapping mechanism for holes (increasing the current) and electrons (decreasing the current) in NMOS transistors and is discussed in [4]. This frequency degradation can be expressed in terms of gate delay, obtaining an estimate of the digital gate time delay degradation with irradiation.

The measured degradation of the ROs frequency will be compared with the ones obtained in HDR tests for quantification of the ELDRS effect. The RO frequency measurements versus TID will be used to calculate gate time delays and extrapolated to 500 Mrad, which is the designed specification of the RD53A chip.

Simulations will be done to estimate which is the maximum delay degradation that this chip and newer versions of it can withstand. The estimates obtained with the extrapolated data at LDR will be compared with simulations to assess the reliability of the chip after high radiation doses at LDR. Chip characteristics dependence on TID will be analysed as well.

5. Summary

The ^{60}Co facility at Ruđer Bošković Institute in Zagreb, along with the LDR irradiation setup were presented. The setup opens the possibility to irradiate integrated circuits in a temperature controlled environment with constant powering and monitoring. It is well suited to study ELDRS, a very important feature of devices built in 65nm CMOS technology that will be operated in the LDR environment of the HL-LHC ATLAS and CMS pixel detectors.

A few RD53A chips were irradiated at the ^{60}Co facility up to 35Mrad of TID. The change of the frequencies of the ROs in the RD53A chips, that corresponds to a change in gate time delay as a function of TID was measured. It will be compared to a degradation measured under HDR conditions and, after being extrapolated to 500 Mrad, will be compared with simulations. The complete analysis will also include results of chip performance parameters degradation study depending on TID and will be published in due time.

6. Acknowledgment

We would like to thank the personnel of the Radiation chemistry and Dosimetry Laboratory of the Ruđer Bošković Institute for operating the source, Igor Sajko, Vlatko Trputec and Svetozar Jančić; as well as Branka Mihaljević, Marija Majer, Marijana Nodilo and Željka Knežević Medija for the permanent support of our experiment and precise dose rate measurements in locations of electronics and samples under study.

We are also grateful to our CERN colleagues: Andromachi Tsirou, Jean-Francois Pernot and Eric Albert for designing, building and helping with the installation of the cold box setup, and Jorgen Christiansen for supporting our experiment.

This work has been partially supported by the Croatian Science Foundation under the project IP-2016-06-3321.

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