

The Readout Electronics of the Mu2e Electromagnetic Calorimeter

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The Mu2e electromagnetic calorimeter has been designed to measure ~ 100 MeV electrons with energy resolution $\sigma E/E < 10\%$, time resolution $\sigma t < 500$ ps and position resolution $\sigma x < 1$ cm. The detector is composed of 1348 un-doped CsI crystals coupled to two large area Silicon Photomultipliers (SiPMs). Each SiPM is connected to a Front End Electronics (FEE) chip which hosts the shaping amplifier and the high voltage linear regulator. A group of 20 FEE is controlled by one Mezzanine Board (MB) which transmits the amplified signals to one Digitizer ReAdout Controller board (DiRAC). The DiRAC samples the waveforms at 200 MHz with 12-bit ADCs, packs the data according to the Mu2e custom format and transmits them to the event builder through an optical transceiver. To limit the number of pass-through connectors and the length of the cables, the readout and digitization electronics is located inside the detector cryostat and close to the interaction target. The boards will have to sustain a neutron fluence of about 5×10^{10} n/cm² @ 1 MeVeq (Si)/y and a Total Ionizing Dose of about 12 krad, while working into a 1T magnetic field and a vacuum of 10^{-4} Torr. This harsh operational environment has made the electronics design challenging and required an extended campaign of tests to select and qualify the employed electronic components. In this paper we report on the board architecture and design, on the qualification of the prototypes, as well as on the results of the first vertical slice test of the Mu2e calorimeter.

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1. Introduction

Mu2e [1] aims to measure the ratio of the rate of the neutrino-less muon to electron coherent conversion in the field of an aluminum nucleus relative to the rate of ordinary muon capture. To achieve this challenging goal, Mu2e will exploit a detector system whose main components are a straw tracker and an electromagnetic calorimeter. The calorimeter [2,3] consists of 1348 un-doped CsI crystals coupled to two large area Silicon Photomultipliers (SiPMs) and arranged in two annular matrices (conventionally named “disks”). Its main role is to provide excellent particle identification capabilities to reject the cosmic muons background, guarantee a fast online trigger and provide useful information to make pattern recognition within the tracker more robust. The tracker and calorimeter are hosted in a cryostat inside a superconductive solenoid and operate in a hostile environment, characterized by a 10^{-4} Torr vacuum, a 1 T magnetic field, and significant radiation fluxes coming from the muon stopping target. The simulation shows that in the inner region of the front disk, expected to be the most exposed to radiation, the Total Ionizing Dose (TID) will reach about 10 krad/year with a neutron fluency $\sim 2 \times 10^{11}$ n/cm²/year.

2. The Readout Electronics

To limit the number of pass-through connectors on the cryostat, the readout electronics system is hosted in custom crates placed on the lateral surface of the calorimeter disks as shown in Figure 1. On the other hand, this solution complicates the electronics design in terms of available space and power dissipation. Furthermore, since the detector will probably be accessible only once a year for maintenance, the reliability and the radiation hardness of the readout electronics are paramount for the successful operation of the Mu2e experiment.

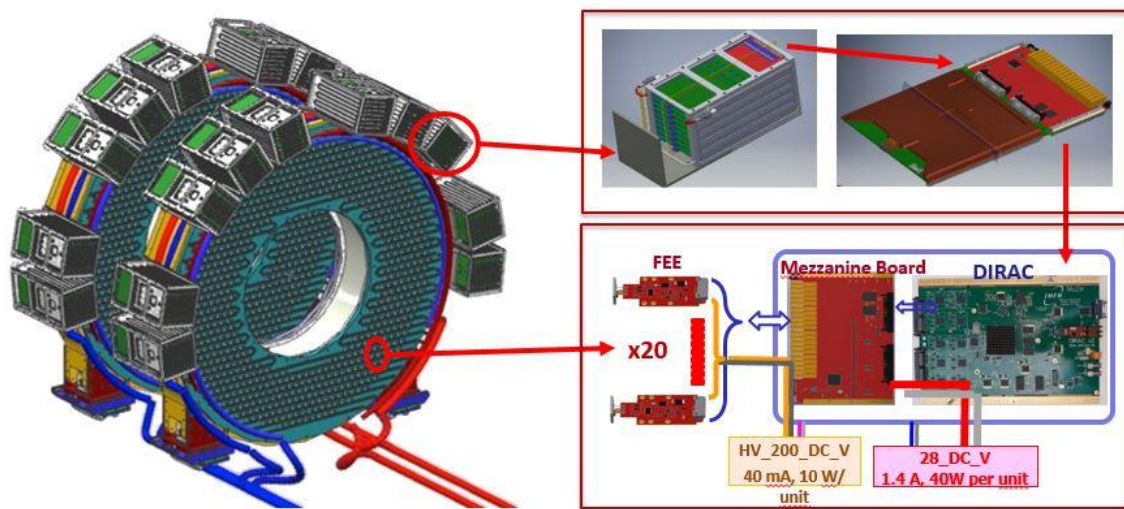


Figure 1- On the left are shown the CAD drawings of the Mu2e electromagnetic calorimeter, while, on the right, are shown the drawings of the electronics custom crate together with a sketch of the readout electronics boards.

The electronics chain is structured as follows: a Front End Electronics (FEE) chip is directly connected to the back of each SiPM to amplify and shape the signals; one dedicated mezzanine board (MB) equipped with an ARM processor controls one group of 20 FEE chips, distributes the low voltage and the high voltage reference values, sets and reads back the locally regulated

voltages; groups of 20 differential signals are sent to the Digitizer ReAdout Controller board (DiRAC) that performs a zero suppression and sends the data packet to the DAQ servers [4] through an optical link.

1.1 Front-End Electronics

The Mu2e Front-End electronics (FEE) integrates a voltage regulator and a preamplifier section on a single board. Each board provides individually programmable biases for each photosensor, performs signal amplification and shaping, while monitoring the current and temperature of each SiPM. Each one of the two SiPMs installed on a single crystal is readout and controlled by a dedicated and independent FEE board. The voltage regulator section has a 1-200 V output range programmable in 50 mV steps. The regulator has a 3 mVpp ripple and a 100 μ s settling time. The transimpedance amplifier section consists of the following stages. Two BJT common-base amplifiers provide low input impedance and are configured as a current summing stage, followed by a low distortion amplifier which in turn drives a pole-zero compensator. Subsequently, the signal is shaped by means of a 3-pole Bessel filter, and finally fed into a balanced differential driver. The shaper provides a 25 ns rise time for the SiPM pulses presented to the digitizer, allowing timing reconstruction algorithms to work with at least 5 sampled points on the leading edge, being the 25 ns rise time five times larger than the digitizer sampling period.

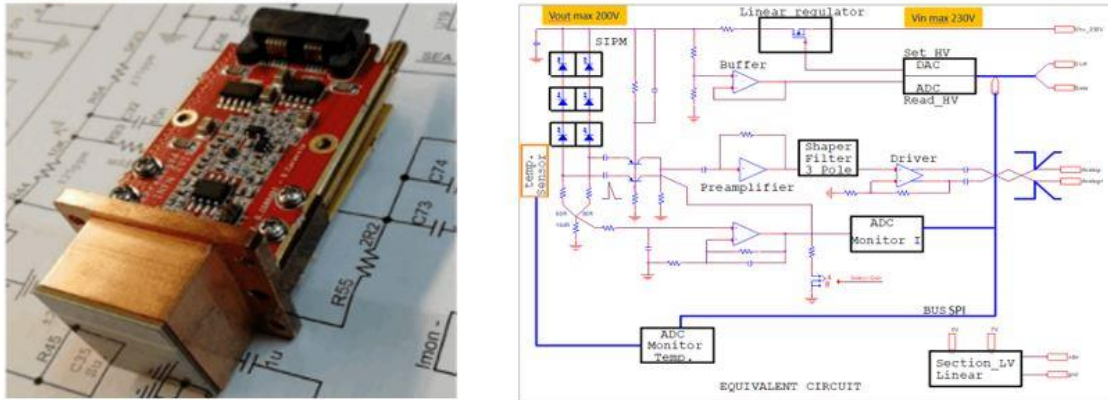


Figure 2 – On the left is shown a picture of a Front End unit composed of 2 SiPMs and 2 FEE chips mounted on a copper cooling structure. On the right is shown the equivalent scheme of the AMP-HV chip.

The mezzanine card (MB) equipped with an ARM processor acts as a bridge between 20 FEE channels and the digitizer (DIRAC). The MB operates a slow control of the channels allowing to set and monitor the bias voltage of the associated SiPMs. Through the MB it is also possible to monitor the current and the temperature of the SiPMs. Furthermore, the MB receives the differential signals from the FEE boards and transmits them to the DIRAC. The communication between MB and DIRAC, which acts as master, takes place via a dedicated I2C interface. The FEE and MB were qualified for usage in the harsh environment of the Mu2e experiment. Samples of the FEE, MB electronics were exposed to gamma irradiation for a TID up to 100, 20 krad respectively, at the Calliope facility of the ENEA Casaccia, Italy. They were also exposed to a neutron flux of up to 3×10^{11} n/cm² at the FNG facility of ENEA Frascati, Italy, and to a proton flux of up to 5.3×10^{10} p/cm² at the North Western Medicine Chicago

Proton Center, Warrenton, USA. Finally, the electronics has been tested in an axial B-Field of 1.5T at Argonne National Laboratory, USA and to dedicated Burn-in tests (FEEs at JINR, Dubna, Russia while the MB at LNF-INFN, Frascati, Italy).

1.2 Waveform Digitizer

The DIRAC-V2 is an evolution of the DIRAC-V1 board [5]. The improvements of DIRAC-V2 derived from the qualification campaign [6] and performance tests carried out on DIRAC-V1. The DIRAC-V2 core is a large FPGA (MicroSemi® Polarfire MPF300) with configuration cells immune to single event upset (SEU). Data coming from 10 ultralow-power double channels 12-bit 250 MHz ADCs (Texas Instruments® ADS4229) are handled by the FPGA. Sparsified and compressed data form packets that are optically transmitted through a fiber transceiver to the Mu2e event builder using a custom protocol. The custom optical transceiver is a bi-directional digital optical data link developed at CERN and named VTRx that operates at rates up to 4.8 Gbit/s and features radiation-resistant (up to 1 Mrad), magnetic field tolerant, low-power and low-mass front-end components. An ultra-low noise jitter cleaner (Texas Instruments® LMK04828) provides a high-performance clock to the FPGA and ADCs, with the option to fine tune relative phases with an accuracy up to 100 ps. The power distribution is handled by 3 DC-DC converters (Texas Instruments® LMZM33606) and 6 LDO (Micrel® MIC69502) to provide rails to the analog components. The DIRAC-V2 board, shown in Figure 3, follows a custom form factor of 233 mm x 165 mm with a thickness of 2.127 mm. The PCB has been designed with 16 layers and has been realized in FR408-HR. All relevant lines have a controlled impedance of 100 Ω for the differential and 50 Ω for single-ended lines. An intense test campaign was performed to qualify all the components to operate reliably in the expected harsh environment. The complete DIRAC-V2 qualification tests included: TID @ENEA Calliope facility with a Co60 source (20 krad), Neutrons @ENEA FNG facility (6×10^{11} n/cm²).



Figure 3 – On the left a picture of the DiRAC-V2 board, while on the right a picture of the experimental setup used to run the vertical slice test: the Module-0 and the crates were hosted inside a vacuum vessel and cooled down with an external chiller.

3. Vertical Slice Test

To verify the performance and the compatibility among the boards that compose the entire electronics chain, a first complete vertical slice test was performed using 20 channels of the so called Module-0 [7], a reduced-scale prototype of the Mu2e calorimeter assembled at the Italian National Institute of Nuclear Physics in Frascati. It is a matrix of 52 crystals and 102 SiPM + FEE units, with the mechanics and the cooling system as similar as possible to the final ones. The test ran with the boards inserted in their custom crates, cooled down with an external chiller and under vacuum. Thousands of cosmic ray events have been collected and used to evaluate the detector performance: the results have been compared with the ones obtained with a commercial CAEN digitizer and showed no significant differences. Since they fully satisfied the Mu2e experimental requirements, the production of the DiRAC board was approved and will be completed within 2022.

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