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The CMS MTD Endcap Timing Layer: Precision Timing with Low Gain Avalanche Diode Sensors

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The MIP Timing Detector of the CMS will provide precision timestamp for all charged particles up to a pseudorapidity of $|\eta| = 3.0$. This upgrade will mitigate the effects of pile-up expected under the High-Luminosity LHC running conditions and bring new and unique capabilities to the CMS detector. The endcap region of the MTD, called the Endcap Timing Layer, will be instrumented with silicon Low-Gain Avalanche Diodes, covering the pseudorapidity region $1.6 < |\eta| < 3.0$. The LGADs will be read out with the ETROC read-out chip, which is being designed for precision timing measurements. We present recent progress in the characterization of LGAD sensors for the ETL and the development of ETROC, including test beam and bench measurements.

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1. The CMS MTD Endcap Timing Layer at High Luminosity LHC

High-Luminosity LHC (HL-LHC), the upgrade of the present LHC, will start operation in 2026. It features an increase of instantaneous luminosity of at least a factor ~ 5, determining the number of 140-200 proton-proton collisions in each bunch crossing. This new harsh environment will cause difficulties in event reconstruction and particle identification due to tracks coming from overlapping vertices. The addition of timing information will make it possible to separate those events overlapped in space but occurring at different moments in time. To this end, the Compact Muon Solenoid (CMS) Collaboration [1] has planned the installation of timing detectors to perform 4D tracking by associating timing information to the reconstructed tracks. In particular, the CMS experiment will be instrumented with the so-called Minimum Ionizing Particles (MIP) Timing Detector [2].

The CMS MIP Timing Detector (MTD) will be made of two parts: (i) the Barrel Timing Layer (BTL), equipped with LYSO crystals read-out by SiPMs, with a total surface of 38 m^2 and hermetic coverage for $|\eta| < 1.45$, and (ii) the Endcap Timing Layer (ETL), instrumented with 14 m^2 of Low-Gain Avalanche Diodes (LGADs) with a dedicated ASIC readout, covering the pseudorapidity region $1.6 < |\eta| < 3.0$. MTD will provide a timing resolution of $\sigma_t \sim 30 - 40\ ps$ at the start of HL-LHC. At the end of lifetime, the resolution in the barrel region will degrade to $\sigma_t \sim 50 - 60\ ps$, while the degradation in the endcaps will be minimal. The detector will improve reconstruction and mitigate the pile-up effect from HL-LHC by collecting timing information on charged particles and combining tracking with timing to assign time information to each reconstructed vertex and track.

The CMS Endcap Timing Layer will comprise two disks for each endcap, mounting silicon sensors on both sides. Its design ensures that 80% of tracks will cross two layers of silicon. Therefore, with a single-hit timing resolution $< 50\ ps$ (which includes both the sensor and readout electronics contributions), ETL will be able to provide a track timing resolution of $\sigma_t < 35\ ps$. To contribute maintaining CMS present performance in HL-LHC environment, ETL will feature:

- a very high fraction of tracks with two timing measurements;
- low occupancy, $< 0.1\%$ at low η and $\sim 1\%$ at highest η, to avoid double hits and ambiguous time assignment;
- radiation tolerance up to fluences of $1.7E15\ n_{eq}/cm^2$ in the inner region (only $\sim 12\%$ of its surface will exceed $1E15\ n_{eq}/cm^2$). To cope with radiation effects, ETL will be operated at a temperature below $-25^{\circ}C$;
- an independent volume, isolated and operated separately from HGCAL, to allow detector maintenance.

2. The sensors for the CMS Endcap Timing Layer

The Endcap Timing Layer will be instrumented with Low-Gain Avalanche Diodes optimized for timing measurements. LGADs are n-in-p Silicon diodes with moderate internal gain. They are provided with a gain layer, a highly-doped thin layer near the p-n junction. This design allows the formation of a high local electric field in the gain layer region, producing charge multiplication.

The gain factor must be moderate, between 10 and 30, to maximize the signal-to-noise ratio.
The requirements for the ETL sensors are the following:

- uniformity of the gain layer,
- fill factor (ratio between active and total detector areas) > 95%,
- low leakage current to limit power consumption and noise,
- large and uniform signals,
- radiation resistance such that the signal has a charge > 8 fC when new and > 5 fC until the end of HL-LHC operation,
- pad size determined by occupancy and read-out electronics.

The sensor active thickness will be $\sim$ 50 μm. Each sensor will be a 16×16 pad array with 1.3×1.3 mm^2 pads. Large-size prototypes have been produced by different vendors, such as Hamamatsu Photonics (HPK) and Fondazione Bruno Kessler (FBK) [3]. R&D studies to define the details for the final ETL sensor design are ongoing, to be finalized by 2022.
Studies of the production uniformity have been performed both on wafer and after dicing. Each wafer in a production has been characterised by measuring the distribution of (i) breakdown voltage for every pad, (ii) leakage current at a fixed bias of every single pad, and (iii) depletion voltage of each pad. The results show that the latest LGAD productions are highly uniform and with low leakage current for both FBK and HPK, well within the required specifications.
Sensor performances in terms of timing resolution have been benchmarked in Beta-source setups based on Sr90 sources in Torino [4] and at Fermilab [5]. The sensors were read out using very fast low-noise electronics. Most prototypes can reach a timing resolution < 40 ps up to fluences of $2.5E15$ n_{eq}/cm^2 (Figure 1).

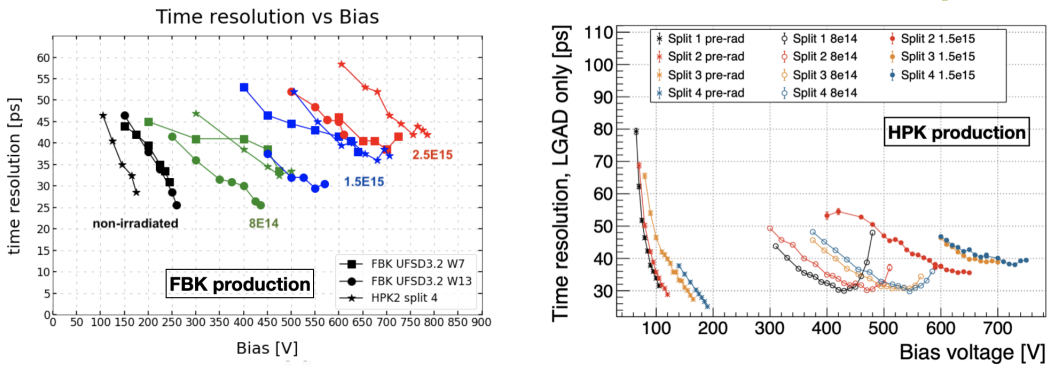

Figure 1: Timing resolution results pre- and post-irradiation for prototypes from FBK (left) and HPK (right) latest productions.

ETL prototypes have also been tested on a 120 GeV/c proton beam at the Fermilab test beam facility. Studies have been performed on a limited number of sensors using a setup instrumented with a strips and pixels telescope for precise tracking, a Photek MCP with 10 ps timing resolution

used as a time reference, an independent scintillator providing the trigger, and an environmental test chamber hosting the LGADs under test. Timing resolution maps have been obtained for new devices demonstrating a uniform $\sim$ 40 ps resolution. Uniform hit efficiency has been observed, reaching $\sim$ 100% in new sensors and $\sim$ 99% after irradiation. Test beam demonstrates that LGADs are highly uniform and efficient, reaching target resolution on large multi-pad arrays [6].

3. ETROC, the ETL read-out ASIC

The Endcap Timing Layer Read-Out Chip (ETROC) is the ETL read-out ASIC. The goal is to reach a timing resolution < 50 ps per single hit on a reduced power budget (1 W/chip, 3 mW/channel). Three prototype versions of ETROC have been planned before the production of the final full-size 16×16 chip: ETROC0, 1 and 2 [7].
ETROC0 is the first prototype, already produced and tested. Its goal is to measure the core front-end analog performance of the amplifier. Jitter measurements agree with chip post-layout simulation, and power consumption for the preamplifier and the discriminator is consistent with expectation. A 31 ps timing resolution has been measured at the test beam at Fermilab with an ETROC0+LGAD system.

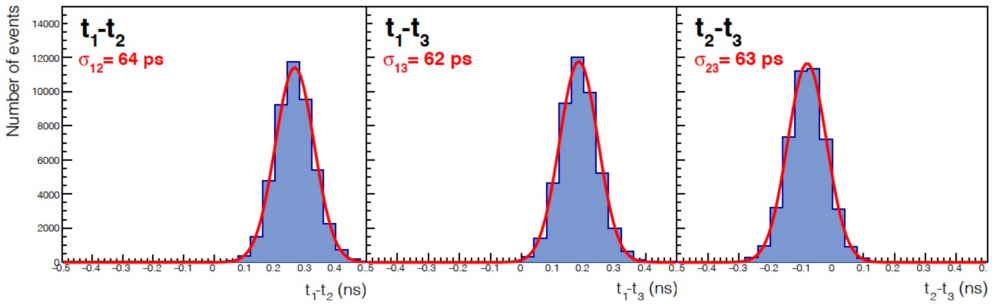

Figure 2: Distributions of time differences between pairs of ETROC1+LGAD layers from the three-layered telescope used at FNAL test beam.

The second prototype version, ETROC1, has 25 channels meant to be bump-bonded to a 5×5 pads sensor, where only 4×4 ETROC channels are used due to H-tree clock distribution. It uses the ETROC0 front-end and includes a new TDC optimized for low power. Low power can be achieved by using simple delay cells with self-calibration. This chip has also been produced and tested. Measurements on the TDC [8] show a resolution of $\sim$ 6 ps. A 40 MHz noise is observed when ETROC1 is bump-bonded with LGADs. This noise is very high and requires a discriminator threshold of $\sim$ 8 fC. It is caused by the 40 MHz clock activity for the circular buffer memory and coupled through the sensor connection to the preamplifier. This issue is under investigation and will be overcome in future prototype chips. Timing resolution measurements have been performed at the Fermilab test beam facility with a telescope provided with three ETROC1+LGAD layers. The aim of these results is to show the timing resolution achievable with large signals. Figure 2 displays distributions of time differences between pairs of telescope layers, where $\sigma_{t_i t_j} = \sqrt{\sigma_{t_i}^2 + \sigma_{t_j}^2}$: as a result, the total time resolution per hit reached for each layer is $\sigma_{t_i} \sim 42 - 46$ ps.

The design of ETROC2 is in progress: it will be a full-size chip with full functionality, and its submission is planned for Spring 2022.

4. Conclusions

The CMS Endcap Timing Layer will perform precise timing measurements of charged particles with single-hit timing resolution $< 50\ ps$ at the start of HL-LHC. This detector will allow the CMS experiment to maintain its excellent performances in the very challenging environment of the High Luminosity era. ETL will be instrumented with thin Low-Gain Avalanche Diodes read out by the dedicated ETROC ASIC.
The latest LGAD productions have been measured both in laboratories and at test beams to ensure they meet the specifications. The sensors are highly uniform, with low leakage currents, good gain, and uniform breakdown voltage. They can reach timing resolutions $< 40\ ps$ up to the end of the HL-LHC lifetime. Test beam results show 100% efficiency and uniform timing resolution across the whole active area of large LGAD multi-pad arrays.
The Endcap Timing Layer Read-Out Chip is required to consume low power while providing excellent timing performances. ETROC0 and ETROC1 prototypes have been already produced and tested, and a timing resolution of $42-46\ ps$ has been measured at the test beam for ETROC1+LGAD. ETROC2 design is in progress.

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