PROCEEDINGS OF SCIENCE

# ATLAS upgrades

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The ATLAS experiment at CERN has planned many upgrades, in order to cope with the instantaneous luminosity that will be delivered by the Large Hadron Collider (LHC) machine in the next decade. These upgrades will allow the ATLAS experiment to keep or improve its current performance for Run 3, expected to start in 2021, and for the High Luminosity LHC program (HL-LHC) expected to start in ~2027. For Run 3, we expect an instantaneous luminosity of 2-3 $\times$ $10^{34}$ $cm^{-2}$ $s^{-1}$ and an average pileup of ~80 collisions/bunch crossing, while for the HL-LHC phase, an instantaneous luminosity of 7.5 $\times$ $10^{34}$ $cm^{-2}$ $s^{-1}$ and an average pileup of ~200 collisions/bunch crossing are foreseen. Although the upgrades are essential to achieve the physics goals, they represent a huge challenge for the detector, trigger and data acquisition (TDAQ) systems. The status of the upgrade activities is presented.

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## 1. Introduction

In the next years, the ATLAS detector [1] will undergo various upgrades, in order to cope with the huge performance foreseen for the LHC machine and to keep its performance at the highest possible level, in terms of acceptable trigger rates at low-$p_T$ thresholds, pile-up mitigation and detector occupancy. It will also have to face the high expected radiation levels (~$10^{16}$ $n_{eq}/cm^2$; ~10 MGy). The upgrade activities will also have to fit the schedule for LHC interventions.

The ATLAS detector has planned two major upgrade programs. The so-called "Phase-I" upgrade program is presently being carried-on and is now reaching its completion, scheduled for mid-2021. The "Phase-II" upgrade program is currently in its final stage of design and R&D. The construction and installation of the Phase-II upgrades is scheduled to take place in the 2025-2027 time frame, and it will prepare the ATLAS detector to take data in the HL-LHC period. The current time line of the LHC upgrades, in preparation for the HL-LHC runs, is presented in Fig. 1. HL-LHC will start to operate in 2027 and will deliver a total integrated luminosity up to 3000 $fb^{-1}$.

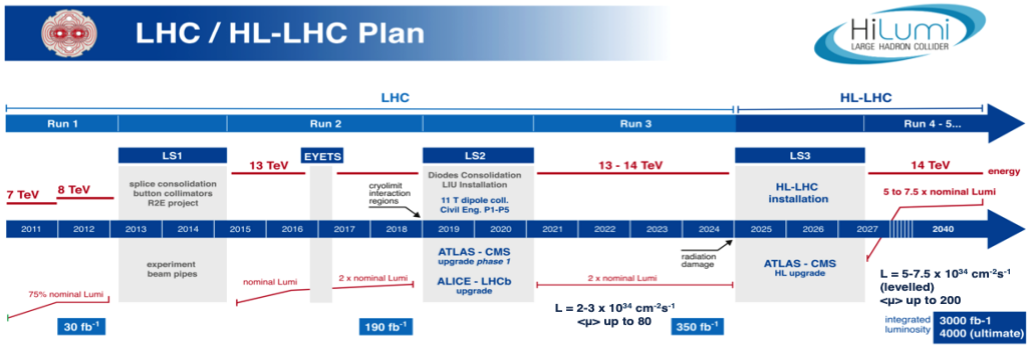


**Figure 1:** LHC schedule for long shutdowns (LS) and luminosity projections through HL-LHC.

## 2. Phase-I upgrade

The ATLAS Phase-I upgrade programme will impact on four areas of the ATLAS detector: the New Small Wheel detector, the liquid argon (LAr) calorimeter front-end electronics, the new muon detectors in the Barrel Inner Small layer and the TDAQ system. A detailed description of the upgrades in each area is presented in the respective technical design reports [2, 3, 4].

### 2.1 The New Small Wheel system

The New Small Wheel system consists of two 5 meter radius wheels (one for the A-side and one for the C-side of the detector) in the end-cap region ($1.3 < |\eta| < 2.7$).

Each wheel is formed by two external small strip thin gap chambers (sTGC) wedges (used mainly for trigger, for bunch crossing identification and for vector tracking) and two internal micromegas wedges (used mainly for tracking with a spatial resolution of less than 100 microns).

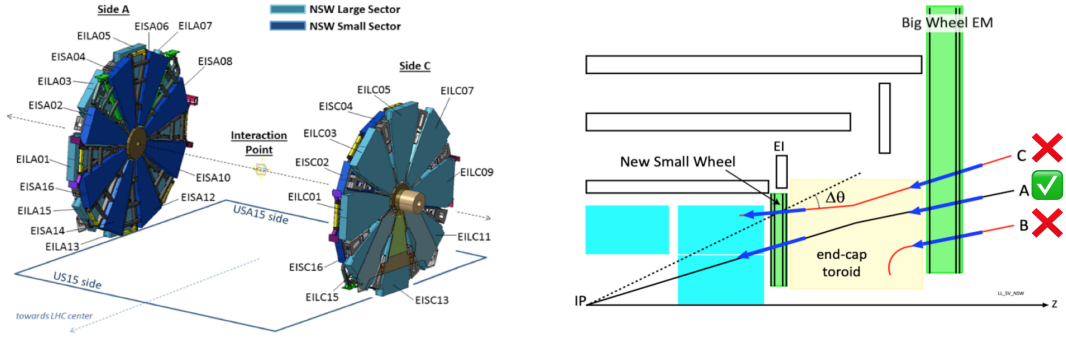


**Figure 2:** Left: the layout of the two New Small Wheels, for large and small sectors. Right: working principle of the track selection trigger of the NSW (transverse view) [2].

The New Small Wheels aim is to reduce the muon triggers caused by noise or accidental coincidences in the end-cap region, by making a coincidence between the existing detectors, the Big Wheel, and the New Small Wheel. As depicted in Fig. 2 (right), only the hypothetical "A" track is accepted, while the "B" track (producing only hits in the Big Wheel) and the "C" track (not pointing to the interaction point) would be rejected. The assembly of the NSW is presently on-going, and the NSW detector is expected to be ready for installation by the end of 2021.

### 2.2 LAr calorimeter front-end electronics

In the LAr calorimeter system, new electronics boards will be installed, in the front-end (*Trigger Digitiser Boards*) and back-end (*Digital Processing Boards*). These upgrades will allow to increase the trigger tower granularity as shown in Fig. 3, improving the granularity from $\Delta\eta\times\Delta\phi = 0.1\times0.1$ to $\Delta\eta\times\Delta\phi = 0.025\times0.1$, and to maintain good trigger performance even at high luminosity and pileup.

Moreover, the calorimeter trigger system (L1 Calo) will be equipped with the new Feature EXtractor boards (FEXs), in order to provide more refined processing of the calorimeter information and to reach a better discrimination between jets, photons, electrons and taus.

The calorimeter upgrade aim is to keep a low trigger rate, thanks to the background rejection, and to keep low thresholds, thanks to the higher geometrical resolution.

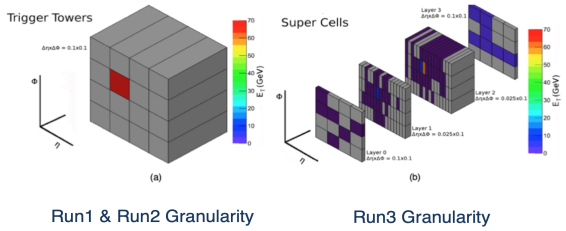


**Figure 3:** Trigger tower granularity increase from Run 1 & Run 2 to Run 3 [3].

### 2.3 Muon detectors in the Barrel Inner Small region

The New Small Wheel will cover the pseudo-rapidity region $1.3 < |\eta| < 2.7$, while the Big Wheel covers a larger region, with $1.0 < |\eta| < 2.7$. Thus, the pseudo-rapidity region $1.0 < |\eta| <$

1.3 is not covered by the New Small Wheel and it is covered only in the large sectors of the muon spectrometer by other existing detectors (EIL4 TGC end-cap trigger chambers).

For this reason, new resistive plate chambers (RPC) detectors will be installed in the Barrel Inner Small (BIS) regions, i.e. only in the small sectors of the muon spectrometer, in order to reduce the foreseen muon trigger rate. The upgrade plan is to replace 16 monitored drift tubes (MDT) chambers with small MDTs, drift tubes with the diameter of 15 mm (instead of 30 mm) and to install 16 new RPC trigger chambers and new front end electronics; the new RPC chambers are updated RPCs, with 1 mm of gas gap, thinner than the ones previously installed, in order to fit in the small space made available by the upgrade of the MTDs. The detector production is ongoing and the installation of the A side should be completed by 2020.

### 2.4 TDAQ system

The ATLAS TDAQ system plans a large number of upgrade activities for Phase-I, in order to keep the trigger rates at sustainable levels and guarantee a smooth data taking, despite the higher number of collisions per bunch crossing. Many parts of the system will be involved in the upgrade process. As an example, we mention:

- the new Sector Logic board for the end-cap: it will receive inputs from new muon detectors (i.e. the New Small Wheel muon system, the RPC BIS) and from the outer layer of the tile calorimeter. All the inputs will be used in order to reduce the trigger rate in the end-cap.

- the L1Topo upgrade, a new board that performs specific topological algorithms on calorimeter and muon data.

- the Central Trigger Processor (CTP), and specifically the new Muon to Central Trigger Processor Interface (MuCTPI) board will manage the data transfers with the new boards (end-cap Sector Logic and L1Topo); it will be based on last generation powerful FPGAs, so as to have more logical resources and higher bandwidth available for data transfers.

- the new readout system will be based on the FELIX (Front End LInk eXchange) system. FELIX is a server-based system that uses custom PCIe cards to interface with the detector electronics, so that it acts like a router between the custom front end links of the various sub-detectors and a commercial multi-gigabit network technology, in order to transfer data to the appropriate destination.

## 3. Phase-II upgrade

The ATLAS Phase-II programme consists of interventions in the following areas of the detector: pixel and strip trackers, LAr and Tile calorimeters, muon system, trigger and data acquisition system. The details of the ATLAS Phase-II upgrades are presented in the technical design reports for each upgrade area [5, 6, 7, 8].

The ATLAS Phase-II upgrades are designed to satisfy the broad ATLAS physics program planned for the HL-LHC phase, especially in order to cope with the high pile-up and data rates running conditions foreseen for Run 4 and Run 5. As an example, for the TDAQ system, it will be crucial to keep the transverse momentum ($p_T$) of the various trigger objects as low as possible.

### 3.1 Pixel and strip Inner Trackers (ITk)

The current ATLAS inner detector was designed to operate for 10 years, at the luminosity of $10^{34}$ cm$^{-2}$ s$^{-1}$ and an average pile-up of 23. The present inner detector would not maintain the needed performance in the harsh environment of the high luminosity.

For this reason, a brand new all silicon tracking system has been designed. It is made of a strip system, covering the pseudo-rapidity region $|\eta| < 2.7$, consisting of 4 barrel layers and 6 end-cap disks, and of a pixel system covering the pseudo-rapidity region $|\eta| < 4$, with 5 barrel layers and inclined modules and rings. Figure 5 shows the layout of the two ITk systems.

The aim of ITk is to reach equal or better performance than the existing detector, in a much more difficult tracking environment: one of the main objectives is to keep a high track reconstruction efficiency (>95%) and a low rate of fake tracks. In order to fulfil these requirements, the pixel system will be composed by more than 10000 modules, more than $10^9$ channels; the strip system will have more than 18000 modules, almost 60 million channels.

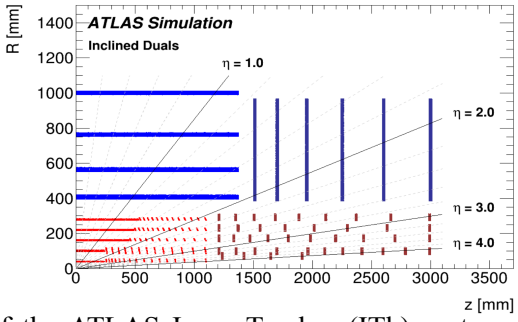


**Figure 5:** Layout of the ATLAS Inner Tracker (ITk) system for Phase-II, showing the strips (blue) and the pixel (red) arrangement [5].

### 3.2 LAr and Tile calorimeters

The current liquid argon calorimeter electronics is not compatible with Phase-II requirements (for latency and trigger rate reasons) and the radiation hardness requirements for Phase-II are above the original design. For this reason, the Phase-I upgrade boards will be kept, but new front-end and back-end electronics will be installed, thus allowing full granularity data to be sent off-detector at 40 MHz.

Moreover, for the Tile Calorimeter, a complete replacement of on-detector and off-detector electronics is foreseen, because of radiation damage and ageing; also the photomultipliers reading out the most exposed cells will be replaced (roughly 10% of the total).

The Phase-II upgraded Tile Calorimeter system will satisfy the HL-LHC radiation requirements and will be compatible with the new TDAQ architecture, being able to transfer full data to the off-detector electronics optically at 40 MHz.

### 3.3 Muon system

The upgrades foreseen for the muons have two main objectives: to reduce the triggers not originating from muon particles in barrel and end-cap regions, and to increase the geometrical coverage in the barrel.

In order to attain these two objectives, new detectors will be installed, specifically:

• in the barrel region:

- in the Small sectors: old BIS MDT detectors will be replaced by new sMDT + RPC (i.e. the same upgrade done in the Muon system for Phase-I);

- in the Large sectors: new RPC detectors will be mounted on top of existing BIL MDT;

• in the end-cap region:

- Thin Gap Chambers (TGC) EIL4 will be replaced by new TGC EIL4 detectors, based on a triplet instead of a doublet, to allow a more robust coincidence algorithm.

The position of the muon detectors for Phase-II is shown in Fig. 6. For the small sectors (left), the coil support structures create trigger coverage holes in the Barrel Middle layer, as it has been for Run 1 and Run 2: these holes will be covered by the new sMDT + RPC detectors planned for Phase-II.

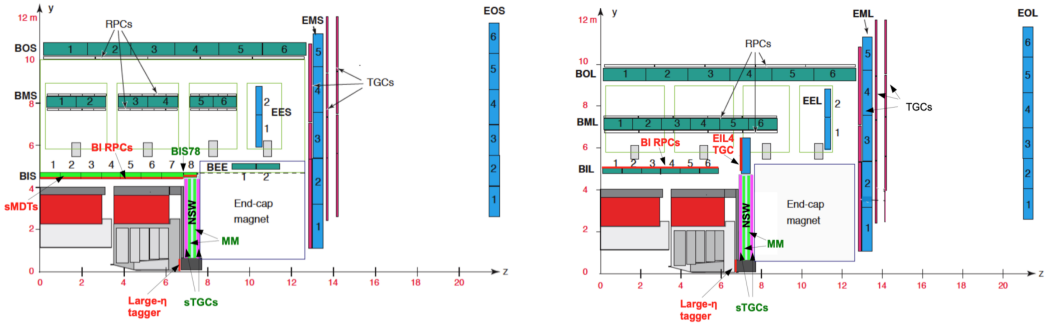


**Figure 6:** The muon detectors installed in the barrel and end-cap region, for the small (left) and large (right) sectors [7].

### 3.4 TDAQ system

TDAQ is made up of three main sub-systems: the Level-0 Trigger, the Data Acquisition (DAQ) and the Event Filter (see Fig.7) and every part will be upgraded for Phase-II.

For the Level-0 Trigger, data from calorimeter (Liquid Argon and Tile) and muon spectrometer (RPC, NSW, TGC) will be provided to the Central Trigger Processor (CTP) that takes the final L0 Accept decision after aligning and combining all the digital trigger inputs. Trigger performance improvements will include both acceptance and momentum resolution.

The DAQ system will be made of the Readout, based on the FELIX system and on the Data Handlers (servers performing detector-specific formatting and monitoring tasks) and the new Dataflow system, that will buffer and transfer data to permanent storage.

The Event Filter system will provide high-level trigger functionality and will consist of a CPU-based processing farm, using algorithms close to offline reconstruction and tracking methods, complemented by Hardware-based Tracking for the Trigger (HTT) co-processors.

The TDAQ Phase-II baseline architecture, based on a single-level hardware trigger with a maximum rate of 1 MHz (it was 100 kHz in Run 1 & 2) and 10 μs latency (it was 2.5 μs in Run 1 & 2), is shown in Fig. 7 (left). The baseline architecture will be capable of evolving to a dual-level hardware trigger architecture, shown in Fig. 7 (right), where the systems in light blue are the additional components, if the evolution will be required (i.e. the hadronic trigger rates and the inner pixel detector layer occupancy are higher than expected).

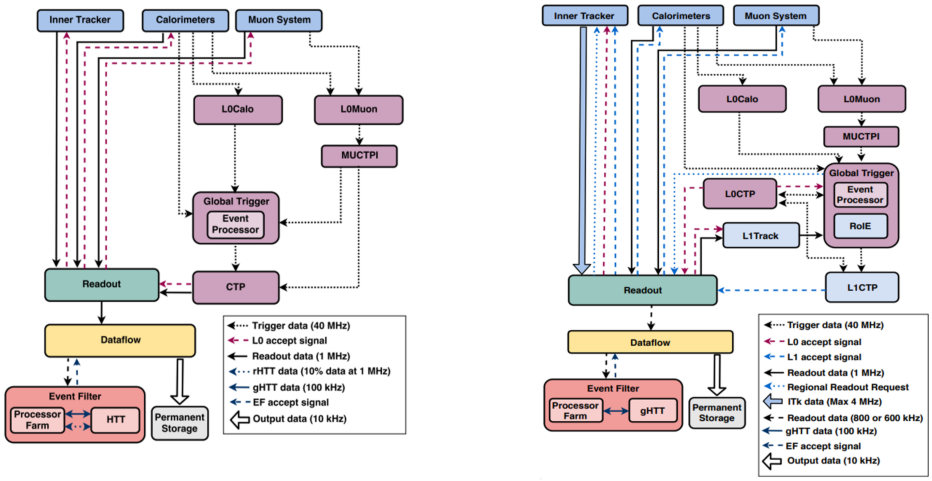


**Figure 7:** TDAQ System in Phase-II: baseline (left) and evolved (right) scenarios [8].

## 4. Conclusion

The ATLAS collaboration has planned a huge upgrade activity, that will allow to fully exploit the LHC physics opportunities until 2035.

The Phase-I upgrade is very well underway. In each upgrade area (calorimeters, muons, TDAQ), many parts of the new systems are being installed and commissioned already in 2020.

The Phase-II upgrade is in the final stage of R&D and current activities are mainly focusing on the production of the first prototypes, following the publication of technical design reports. The main activities will be on the new tracker and new calorimeters, in order to improve the pile-up handling, and on muons and TDAQ system, in order to increase trigger and readout capabilities.

## References

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