

Muon trigger using deep neural networks accelerated by FPGAs

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Accuracy and latency are crucial to the trigger system in high luminosity particle physics experiments. We investigate the usage of deep neural networks (DNN) to improve the accuracy of the muon track segment reconstruction process at the trigger level. Track segments, made by hits within a detector module, are the initial partial reconstructed objects which are the typical building blocks for muon triggers. Currently, these segments are coarsely reconstructed on FPGAs to keep the latency manageable. DNNs are ideal for these types of pattern recognition problems, and so we examine the potential for DNN based track segment reconstruction to be accelerated by dedicated FPGAs to improve both processing speed and accuracy for the trigger system.

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Figure 1: Visualization of the chamber with all hits in 1a and its CNN prediction 1b by 1c

1. Introduction

Recently, a boosted decision tree (BDT) has been successfully implemented into the CMS endcap muon track finder trigger using an FPGA implementation [1]. The BDT was used to assign transverse momentum on muon trigger objects, which is a collection of segments from multiple detector modules (chambers), showing great improvements over the previous look up table method [2]. We aim to improve similar tracking based triggers by improving the segments. Segments are a collection of hits within one detector modules or chambers that represent a partial track. We implement a convolutional neural network (CNN) to improve the segment making process.

2. CNN based Reconstruction in FPGA

We use GEANT4 [3] to simulate a muon detector chamber similar to [4], consisting of 6 layers in the z-axis, with each layer consisting of 384 strips in the x-axis and segmented in 8 partitions in the y-axis.

The aim is to train the CNN to only reconstruct the muon segments which are marked as blue points in Fig. 1a and then accelerating the CNN inference by FPGA. Because of the restriction of layers in FPGA DPU Architecture, 2D Depthwise Separable Convolution is used to learn the relation on channel axis direction [5] [6] [7]. The model is trained in the tensorflow.keras framework, and the structure is given in 1c. [8]

Xilinx Alveo U250 FPGA is used for inference acceleration. The weights of the CNN are quantized by changing 32 bit float to 8 bit integer, in order to save memory usage and reduce latency [9].

3. Results

Efficiency and fake rate are used to evaluate the model, as shown in Fig. 2. The efficiency is defined as the number of matched images divided by the number of images containing muons, and the fake rate as the fraction of the number of wrong reconstructed hits. Fig 2c shows the throughput which is used to benchmark the latency of various platforms and it is measured as processed images per seconds (FPS), includes data transferring delays. The performance is very promising, showing very high efficiency with the fake rate low and with even lower latency.



Figure 2: (a): Efficiency (b): Fake rate (c): Throughput as a function of batch size is 1, 2, ..., 2048.

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