

Upstream Tracker - The silicon strip tracking detector for the LHCb Upgrade

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After operating for 10 years, the LHCb detector at the LHC is currently undergoing a major upgrade. New tracking detectors will be installed to improve tracking performance and to allow taking data at higher instantaneous luminosity than in previous runs. Front-end readout electronics of all subsystems is being replaced by boards with readout at collision frequency of 40 MHz. That will allow application of software-only trigger and prompt data analysis techniques.

The Upstream Tracker (UT) will be located in the fringe field in front of the LHCb spectrometer magnet and will be composed of four layers of silicon strip sensors. Custom hybrid flexible circuits and front-end readout chip, SALT, were developed for powering and processing measured signals and to transfer them to the near-detector electronics.

This contribution describes the design of UT components, their novel features and detector performance measured during system tests. The current status of installation and commissioning plans are also given.

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1. Introduction

The LHCb detector is undergoing a major upgrade during the LHC long shutdown 2 in 2019–2021 [1]. The aim is to run at a 5-times higher instantaneous luminosity than in previous run periods (target of 2×10^{33} cm⁻²s⁻¹), keeping the tracking performance the same or improving on what was achieved with the previous detector and reading out all detectors at 40 MHz frequency.

All three tracking detectors will be exchanged: the Vertex Locator (VELO) will be based on silicon pixel instead of strip detector, the Upstream Tracker (UT) that will be installed in front of the spectrometer magnet will use silicon micro-strip sensors, and SciFi tracker installed behind magnet will use scintillating fibres read out by silicon photomultipliers. Other changes include replacement of optics and photodetectors of RICH detectors and removal of detectors that were installed in front of electromagnetic calorimeter (PreShower, Scintillating Pad Detector and first muon station M1).

The UT will play an important role in the tracking at trigger level: by requiring a hit in the UT in addition to VELO and SciFi, the p_T resolution improves and the number of fake tracks decreases to about one fourth. Furthermore, by matching track segments in VELO and UT, very low- p_T tracks can be removed and the hit search window in SciFi will be tightened, allowing for a trigger speedup.

2. UT components

UT will consist of four planar detection layers covering the full acceptance of the experiment. The first and the last plane will have modules with vertical strips, the two intermediate planes will have strips rotated by $\pm 5^{\circ}$. Each detector plane will cover approximately $2 m^2$ and will be built from



Figure 1: (left) Schematic layout of the UT modules (rectangles) and their organisation in planes and staves. The rectangle colour represents sensor type: type A (green), B (yellow), C and D (pink) [1]. (right) Module and flex arrangement on a stave.

Sensor type	Junction	Thickness	Strip pitch	Length	Strips	# sensors
А	p-in-n	320 µm	187.5 µm	99.5 mm	512	888
В	n-in-p	250 µm	93.5 µm	99.5 mm	1024	48
С	n-in-p	250 µm	93.5 µm	50 mm	1024	16
D	n-in-p	250 µm	93.5 µm	50 mm	1024	16

Table 1: UT sensor properties.



Figure 2: Design features of UT sensors: embedded pitch adapter used for A-type sensors (left), top-side high voltage (center) and circular cut-out of D-type sensors to accomodate the beampipe (right).

staves which carry sensors and readout hybrids as shown in Figure 1. The sensors will be mounted on both stave sides in such a way that there will be a small overlap between neighbouring sensors.

Compared to the previous detector, Tracker Turicensis (TT), the UT will have finer granularity, full tracking coverage in the LHCb acceptance and will reduce the beampipe clearance by a circular opening in the sensors around the beampipe.

Sensors

Four different sensor designs listed in Table 1 will be used to cope with varying track occupancy and radiation dose. The majority of sensors, referred to as type A, are approximately 10 cm x 10 cm, *p-in-n* type sensors with 512 strips. To facilitate wire bonding of strips to readout chips, these sensors have an embedded pitch adapter near the edge of the active area.

Sensors in the inner-most area will have a finer segmentation (type B, C, D) and shorter strip length (type C and D) because of larger track occupancy. Due to higher radiation dose, thinner *n-in-p* sensors will be used. Sensors of the D type will have a circular cut-out to extend the tracking coverage around the beampipe. The bias voltage for all modules will be applied via top-side contact. These features are shown in Figure 2. Non-irradiated and irradiated sensors implementing them were tested with beam and no significant degradation of the signal-to-noise ratio was observed above the depletion voltage [2, 3].

Readout chips

A new radiation-hard front end readout chip, SALT (Silicon ASIC for LHCb Tracking) [4], has been developed for the UT. It is based on 130 nm technology and it can sample signals at the design frequency of 40 MHz. Each chip has 128 input channels and incorporates pre-amplifier, shaper, 6-bit ADC (5-bit and polarity bit), pedestal and common-mode noise subtraction, zero suppression and serialization. The resulting digital signal is sent via flex cable to near-detector electronics.



Figure 3: (left) Module built from type A sensor and hybrid circuit carrying 4 SALT chips. The left part of hybrid is used during testing and is cut off before gluing on stave. (right) UT readout chip glued on hybrid and wire-bonded to type A sensor; embedded pitch adapters are also clearly visible.

Modules and staves

The silicon sensors and hybrid flex circuits carrying 4 or 8 chips will be integrated into modules as shown in Figure 3. Modules will be mounted on staves, lightweight carbon-fibre support structures with integrated titanium pipe for CO_2 evaporative cooling. There will be 68 staves in total, each with fourteen to sixteen modules.

Power, bias voltage and signals will be supplied to modules via Kapton flex cables. Each of these provides power and readout for up to 24 chips, what translates to 120 high-speed differential pairs, total current of 8 A and bias voltage for 4 modules. The total thickness of flex is $360 \,\mu\text{m}$, with 22.5-34 μm thick copper traces.

Near-detector electronics and services

The top and bottom of detector frame will house crates of Data Control Boards (DCB) which will be connected to staves via flex cables ("pigtails"). On each DCB there will be 7 GBTx chips for data processing and one GBT-SCA chip [5, 6] which uses I2C protocol for SALT controls and monitoring. Each DCB will have four mezzanines with Versatile Link optical transceiver and connects to 8 optic fibres for readout, clock distribution and controls.

The staves will be mounted in a detector box which will also house manifolds of CO_2 evaporative cooling. To allow opening of the detector during beampipe bakeout, the detector boxes will be openable. Four cable chains will carry cables, optic fibers and pipes. The low-voltage regulators will be installed in crates fixed to the magnet yoke, about 4.5 m away from the beampipe, translating into up to ~10 m of cable between regulators and modules.

3. System tests

A setup to test prototype components, with near-final powering and readout electronics, was built at CERN in 2019. It allows to test one UT stave at temperatures from -30°C to 20°C and evaluate its performance and long-term stability. An example of a noise measurement for one chip is shown in Figure 4. The noise is consistent with values measured in single-module setup during module construction. The setup was also used to validate mounting procedures and for development of control and monitoring software.



Figure 4: Noise measurement of Chip 0, module S1 on stave 5 (longest flex cable path) with non-irradiated sensor at 5° C and 400 V bias voltage. The first two plots show noise in 128 strips before and after trim DAC and pedestal correction. The right plot shows values of total (red) and common-mode subtracted noise (blue). The expected signal amplitude for minimum ionizing particle is about 13 ADC counts, giving signal to noise ratio of ~15.

4. Current status and outlook

The production of UT is ongoing at institutes and at CERN. However, all sites were impacted by the current pandemic situation and the progress has slowed down.

All sensors have been manufactured by Hamamatsu Photonics and tested. About 700 out of 888 A-type modules were built and tested and the stave production is on schedule. All near-detector electronics was produced and burned in and about 80% of the final QA tests were finished. The infrastructure (cabling, auxiliary patch panels and boards) is being produced. After assembly and testing of the UT in cleanroom, the aim is to install the detector underground in fall 2021.

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References

- LHCb collaboration, LHCb Tracker Upgrade Technical Design Report, CERN-LHCC-2014-001, CERN, Geneva, 2014.
- [2] A. Abba et al., *Testbeam studies of pre-prototype silicon strip sensors for the LHCb UT upgrade project*, NIM A806 (2016) 244, arXiv:1506.00229 [physics.ins-det].
- [3] M. Artuso et al., *First beam test of UT sensors with the SALT 3.0 readout ASIC*, LHCb-PUB-2019-009, 2019.
- [4] S. Bugiel et al., SALT, a dedicated readout chip for high precision tracking silicon strip detectors at the LHCb Upgrade, JINST 11 (2016) 02, C02028.
- [5] P. Moreira et al., *The GBT Project*, TWEPP 2009 proceedings, DOI: 10.5170/CERN-2009-006.342, 2009.
- [6] K. Wyllie et al., *Electronics architecture of the LHCb Upgrade*, LHCb-PUB-2011-011, https://cds.cern.ch/record/1340939/, 2011.