Implementation of large imaging calorimeters

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The next generation of collider detectors will make full use of Particle Flow algorithms, requiring high precision tracking and imaging calorimeters. Featuring a granularity by 2 to 3 orders of magnitude higher than existing devices, imaging calorimetry has been developed during the past 15 years by the CALICE collaboration and is now reaching maturity. The state-of-the-art status and the remaining challenges are reviewed here for all investigated sensor types: silicon diode and scintillator for electromagnetic calorimeters, gaseous with semi-digital readout, and scintillator with SiPM readout for hadronic ones. An overview of recent commissioning and beam test results of large-scale technological prototypes and raw performances such as energy resolution, linearity, and studies exploiting the distinct features of granular calorimeters regarding pattern recognition is presented. Beyond these prototypes, the design of experiments addressing the requirements and potential of imaging calorimetry is discussed.

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1. Introduction

The next collider is likely to be an e^+e^- Higgs factory, with centre-of-mass collisions around 250 GeV. All of the current projects – ILC, CLIC, CEPC, FCC-ee – envisage achieving the required precision in the reconstruction of the di-jets final state by the use of the Particle Flow approach combining the information from a high-precision tracking system and ultra-granular calorimeters, and the use of algorithms imaging the contributions of individual particles.

The pioneering ILC detector concepts, SiD and especially ILD[1], have since been adapted to the other projects (CLICdet [2], CEPC-baseline [3], FCC-ee CLD [4]). Beyond the standard requirements, their calorimeters present extremely high granularity and density, allowing compact showers; typical parameters for the electromagnetic and hadronic calorimeters (ECAL and HCAL, respectively) are summarized in table 1.

Table 1: Global scaling parameters of the imaging calorimeters envisaged for the future Higgs factories experiments SiD, ILD, CLD, CLICdet, CEPC-baseline with (Si)licon, (Sc)intillator and (Gas) options.

	Barrel (R) and End-Cap (Z) distances to IP	*Thickness*	*Lateral cell size*	*Number of layers*	*Cell density*	*Total Number of Cells*
ECAL	R = 150–200 cm, $\lvert Z \rvert$ = 200 cm	25 cm / 22–26 X_0	0.5×0.5 cm² (Si) 0.5×4.5 cm² (Sc)	26–40	3-4k /ℓ (Si) 300/ℓ (Sc)	40M–80M 10M (Sc)
HCAL	*ECAL end* + 3 cm	~160 cm / 4,5–7.5 λ_I	1×1 cm² (Gas) 3×3 cm² (Sc)	40–60	500/ℓ (Gas) 55/ℓ (Sc)	50–70M (Gas) 4M–9M(Sc)

Imaging calorimeters face many technical challenges: the density of cells imposes the use of low-power embedded electronics, if possible eluding the use of active cooling; a large number of elements calls for scalability and semi-industrialised production, while the compactness and uniformity require minimal dead spaces and the integration of absorber in the supporting structure. The CALICE collaboration has been put together to address all of these technical issues by building and testing realistic, so-called technological prototypes.

2. Front-End Electronics

The prototypes described in the following sections, SiW-ECAL, ScW-ECAL, AHCAL, and SDHCAL, share a common set of ASICs developed by the Ωmega group; the ASICs vary in their analog parts adapted for SiPM, Silicon or RPC readout, but are fairly identical concerning their storage and digital parts. This allows for gradual improvements and cross-developments.

The ASIC's outputs are purely digital and designed to be daisy-chained to minimize the cabling. Their operation is adapted to ILC conditions, featuring a low-power consumption using power-pulsing at 1% (~ 2 ms at 5 Hz), low-noise pre-amplification, eventually dual-gain 12-bits ADCs and ns-precision TDC, self-trigger with local analogue storage, delayed digitization and readout, and high integration (36–64 channels). The current versions of the ASICs will require to be updated for final ILC integration in order to achieve full zero-suppression, single ASIC addressing, and a switch to a new technology[1]. Such developments usually take 3 to 4 years. Moreover, the studies for the CMS-HGCAL have highlighted the potential of improved timing

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[1]probably CMOS 65 or 130 nm as the current AMS SiGe 0.35μm technology is soon to be discontinued.

measurement for particle identification and particle flow reconstruction. A compromise between the timing precision and the power consumption will have to be established.

For circular colliders, the optimal working points, balancing precision, power, and readout speed need to be established; this might be done dynamically through the ASIC configuration to fulfill the wide range of running conditions.

3. Technical requirement on technological prototypes & common goals

The practical constraints arising from building and operating large detectors translate into the use of connected detectors elements made of a PCB carrying the sensors and the readout ASICs and integrated into cassettes of up to 150–300 cm long for 12k to 27k cells (200–500 ASICs). They must operate in power-pulsed mode while keeping a good sensitivity to mip[2] signal and a reasonable uniformity, stability, and linearity in a 3 to 4T field. The cassettes will be read at a single end, where a single interface will ensure their powering and cooling, piloting and monitoring; in the detectors, the power budget and space available will be minimal, with an ECAL–HCAL gap of only 3 cm, roughly doubled for the HCAL–Coil or Barrel–Endcap transitions.

The validation of the design is twofold, technical and scientific.

The technical goals are a scalable design operating with power-pulsing[3] with good uniformity and linearity performances, and the input for realistic detector simulation. The devices are first tested off-beam to remove or mask problematic cells. In-beam, spatial scans with mips (muons or electrons, once the absorbers are removed) provide low-energy calibrations and noise maps. The signal-to-noise ratio (S/N), defined as the position of the Most-Probable-Value of a mip to the noise standard deviation (MPV/σ), for the trigger branch of the ASIC's is critical, as it impacts directly their limited memory capacities and their capacity to record further events. The low-energy response indicates uniformity and efficiency through the mean response to mips (expressed as light yield, mip MPV peak, multiplicity respectively for scintillators, silicon, and RPC sensors). Averaged calibration and noise maps, completed with the high-energy limitations such as saturations and non-linearities, are the inputs to realistic digitization models, mandatory for the prototype and Particle Flow simulations in the full detectors. Several development cycles have been necessary to improve the critical elements' design and noise performances (Sensors, PCB, ASICs).

The scientific goals encompass the classical energy and time measurements of single particles: the linearity and resolution of the response to single muons and electrons and pions in the 1–200 GeV range. The measurements of 5D shower profiles (spatial plus energy and time) is also an area of improvement for Monte-Carlo's. Finally, the performance of PFA – shower separation, reconstruction, identification – can be tested on real data by the software overlapping or neutralizing of particles. This work extends the one done on the "physical prototypes" (excluding many of the technological constraints) presented in these proceedings [5].

Finally, the design's reproducibility testing will only be achieved by building 20–50 cassettes, a minute fraction of the 10^4 foreseen for the detectors.

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[2] Depending on the context "mip" stands here for *minimum ionising particle*, or the signal level produced by such particles crossing a sensor perpendicularly; in practise punch-through electrons, pions and muons are not distinguished.
[3] The prototypes are usually operated in a pulsing mode as close as possible to the ILC mode (200 ns bunch-crossing repeated at 5 Hz) but might be set in a relaxed mode for practical reasons (typically 4 μs bunch-crossing).

4. Silicon-Tungsten ECAL (SiW-ECAL)

The SiW-ECAL is built from detector elements of 18×18 cm², for 1024-channel, equipped with SKIROC2 & 2a ASICs. Their testing has demonstrated most of the technical goals (at the exclusion of the power dissipation[4]), with a S/N = 11.6±0.7 (for 10 demanded) on single detector elements and pulsed operation in a 1 T magnetic field. This allows for triggering at a 1/3 mip MPV with nearly 100% efficiency while keeping noise cut at 4 σ. A recent improvement in PCB design increased the S/N in the readout branch from 16–17 (with 320 μm wafers on PCB version v11) to 20.3 ± 1.5, while the number of masked channels went from 8 % to 0.3% [6]. This ratio rises to 30–40 when using 650 μm wafers on the latest PCB version (v13). A thin version with the ASIC directly bounded onto the PCB is also investigated.

Since 2016, the technological prototype, stacking single detector elements interleaved with tungsten absorbers, has been continuously expanded; in 2020, it groups 15+7 single elements, mixing 4 PCB versions (v10 to v13), carrying packaged and onboard ASIC's, on which 320, 500 or 650 μm-thick silicon sensors are glued. A new compact readout in line with the space requirement for the ILD ECAL (3 cm clearance) has been designed and implemented [7]. It handles 15 layers (15,360 cells) in a single readout. After the COVID-related cancellation of 2020 beam test campaigns, new ones at DESY and CERN are foreseen in 2021.

The ILD-design single-ended readout imposes the building of cassette lining up to 8 to 12 (barrel/end-caps) detector elements; in 2018, a simplified "electric" prototype of 8 elements, each equipped with a single "baby-wafers" (2×2 cm², 320 μm, 16 ch), was operated in-beam. The response to punch-through electrons has shown comparable and uniform S/N as for the individual elements. A drop in the response of ~10% along the cassette length was attributed equally to in-line power losses and the ASIC's reference voltage variability [8]. Both are to be corrected in the next versions of the ASIC and PCB.

5. Scintillator-Tungsten ECAL (ScW-ECAL)

ILD and CEPC-baseline detector envisage an ECAL based on scintillator strips [9], measured by SiPM's soldered onto a PCB, rotating by 90° between each layer. A technological prototype is being finalised; 32 layers, 210 channels each, are in tests both for aging (curing for 48h at 50°C) and for calibration. The sensor layers are interleaved with 3.2 mm of Cu-W (15%/85%) alloy for a total thickness of 9.2 mm per layer. The version 2e of the SPIROC ASIC is used. Thirty layers have 45 mm strips, readout by a single SiPM, while two layers test 90 mm strips with 2 SiPM. Two types of SiPM are used: HPK S12571–010P, featuring 10k pixels and 10 μm pitch as a baseline (24 layers), and an alternative with a 15 μm pitch (6 layers). The first yields a dark count (>0.5 p.e.) of 100 kHz at nominal voltage, and can count up to 15,000 photons with an uncertainty of 3% after correction for statistical misses.

A clear separation of a mip signal is observed in the self-trigger mode for cosmic rays and from 90Sr source. The MPV position typically varies of 16–17 % among strips. The prototype is likely to be ready for in-beam operation at the beginning of 2021.

The R&D focuses on improving the uniformity response of strips. An interface between the SiPM and the scintillator-strip designed as a centred groove with the shape of a race-track

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[4]Each ASIC handles 64 channels, with theoretical power of 25 μW/ch for a 1% power cycle; practically, a factor of 5 to 10 is still to be gained.

minimises the non-uniformity of the signal along the strip length down to 4 %, when measured by a scan of a 90Sr source.

6. Scintillator AHCAL

The AHCAL features square scintillator tiles, measured by a SiPM directly mounted on a PCB in two configurations suitable for ILD at ILC [10] and the CMS-HGCAL at the HL-LHC. Since 2017, a technological prototype supersedes a mixed physics prototype[5]. Now, 38 uniform squared layers of 72×72 cm² are segmented in 576 moulded tiles (eventually complemented by six layers with coarser granularity), each readout by 16 Ωmega SPIROC2e ASICs, and interleaved with 1.7 cm thick stainless steel plates (for a total of ~ 4 λ_I and 22k channels). After a series of stand-alone beam tests, the AHCAL prototype was operated in 2018 in synchronisation with the CMS-HGCAL Silicon ECAL and HCAL parts. The beam test will continue with a tungsten structure build for AIDA [11], already used for the physics prototype.

The SiPM gain variations to temperature and voltage changes are dynamically corrected. The statistical saturation occurring for single-cell deposits $E_{hit} \geq 100$ mips (when the number of photon-electrons approaches the number of pixels) is now corrected for up to 350 mips.

The time dimension will complement the previous analyses on shower profiles and PFA tests, helping out shower start determination, particle identification, and neutronic component determination. The first step of calibration has started using beam muons; the SPIROC2e ASIC time slopes, feeding the ADC for odd and even bunch-crossings, are equalized, yielding a time resolution of 2.6 ns for a 250 kHz (beam-test mode), going down to 1.6 ns at 5 MHz (ILC mode), and narrowing to the 1 ns goal for the ILC detectors.

R&D for mass production is pursued in 3 directions: "MegaTiles," large scintillator tiles with trenches every 3 cm, are expected to ease considerably the building of large detectors. In the 2019 beam tests, the light yield, mip response, and optical cross-talk were evaluated. A larger cross-talk in beam than in cosmics was attributed to different mechanical constraints, corrected for and tested in August 2020. The second direction is determining the tiles' needed relative positioning precision to the SiPM, using a collimated source. The measurements will also help in making the simulation more realistic. Finally, a "long layer" is being built: a table-top layout works appropriately with three connected technological prototype layers. The ILD requires to increase its length by 50 %, and then to place test it in a beam.

After some tests with the SPIROC2e, the first board using the HGROCv3 ASIC for the CMS-HGCAL has been produced and tested at DESY in summer 2020.

7. SDHCAL: Semi-Digital Gaseous HCAL

A technological prototype of the SDHCAL [12] was built in 2011, including single and multi-gap thin GRPC[6], segmented in cells of 1×1 cm² and separated by 2.6 cm stainless-steel absorbers. Ωmega's HARDROC2 ASICs perform the readout. The prototype has 48 layers of 1×1 m², 460,000 cells spanning 6 λ_I.

For this semi-digital calorimetry, the energy is classified by three thresholds. The uniformity of the response is estimated by the efficiency and multiplicity of cells above the lowest

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[5] used from 2006 to 2011 and mixing tiles of 3×3, 6×6, and 12×12 cm²
[6] Gas Resistive Plate Chamber

threshold. The optimal energy response to a single particle (e, π, p) requires threshold optimisations (typically at 1/2, 5 and 15 mips) done by dedicated scans and hit counting mitigation [5]. A good description of the data by simulation has now been achieved up to 40 GeV for electrons and pions by modelling many overlapping effects in avalanches, readout, and time.

The future developments for large detectors focus on large cassettes of 3×1 m², with an improved HARDROC3 ASIC implementing I2C addressing, full zero-suppression, and a tripled dynamic range, up to 50 pC. Large and uniform GRPC's design is being experimented with optimal gas-flow, on which larger PCB (32×96 cm²) with fewer connectors are glued. An electron beam-welding structure for a couple of cassettes is now ready.

Longer-term R&D aims at improving the timing measurement in every cell using low jitter Ωmega PETIROC ASIC (20 ps) and Multi-gap GRPC (60 ps) to reach a precision below 100 ps.

8. Conclusions

The technological prototypes for the four main sensor-options of CALICE are have been extensively in (HCAL's) or are getting ready for (ECAL's) large beam-test campaigns to provide comparisons within the ILC timeline (≤ 5 years of R&D). They will provide a wealth of information on digital calorimetry, in-shower software compensations, new particle ID variables, timing in calorimeters, and a fertile ground for new analysis techniques. Besides large prototypes, many small scale R&D are taking place to explore new ideas, model technology and physic's specific needs.

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