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Upgrade of the CMS Cathode Strip Chambers for the HL-LHC

Sven Dildick[†] *

Rice University,
6100 Main Street, Houston, TX 77005, United States

E-mail: sven.dildick@cern.ch

The Large Hadron Collider will be upgraded in several phases to significantly expand its physics program, and these upgrades present major challenges to the operations of the Compact Muon Solenoid cathode-strip-chamber muon system. After the current Long Shutdown (LS2) from 2019-2021 the accelerator luminosity will be increased to $2-3\times10^{34}$ cm^{-2} s^{-1}, exceeding the design value of 10^{34} cm^{-2} s^{-1} and allowing the CMS experiment to collect an integrated luminosity of approximately 100 fb^{-1}/year. A subsequent upgrade in 2024-2027 will increase the luminosity up to $5-7.5\times10^{34}$ cm^{-2} s^{-1}. The CMS Muon system must be able to sustain a physics program after the LS2 shutdown that maintains sensitivity to electroweak scale physics and for TeV-scale searches. The CSC upgrade program is designed to address key challenges associated with operations at high luminosity. The electronics will be upgraded to handle the expected higher data rates. The design of the upgraded CSC electronics will be discussed, as well as the status of the first phase of the electronics installation. In addition, accelerated irradiation tests are being performed to study the behavior of the CSC electronics under conditions, which are nearly an order of magnitude beyond the original design values. Studies have also been performed of chamber gas mixtures to reduce greenhouse-gas impacts. The status of this irradiation campaign and results will be presented.

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[†]On behalf of the CMS Collaboration
*Speaker

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1. Introduction

The Compact Muon Solenoid (CMS) experiment [1] is one of the general-purpose experiments at the CERN Large Hadron Collider (LHC). The CMS detector uses three complementary systems to detect muons. Drift Tubes (DTs) are installed in the barrel region, (pseudo-rapidity $0 < |\eta| < 1.2$), Cathode Strip Chambers (CSCs) in the endcap region ($0.9 < |\eta| < 2.4$), and Resistive Plate Chambers (RPC) in both the barrel and endcap regions ($0 < |\eta| < 1.8$). The locations of these detectors are shown in Fig. 1 (left). During the second Long Shutdown (LS2) and Run-3, new Gas Electron Multiplier (GEM) chambers will be installed in the forward region ($1.6 < |\eta| < 2.8$). The RPC coverage will be increased to $|\eta| < 2.4$ with improved RPCs (iRPC) [2].

CSCs are trapezoidal gas proportional chambers with both a cathode-strip and anode-wire readout. A chamber has seven layers forming six gas gaps, each 9.5 mm thick, filled with an $Ar/CO_2/CF_4$ mixture and placed under high-voltage. A total of 540 CSCs are installed in four stations in two endcaps. Each CSC has a finely segmented readout, which provides a time resolution of ≈ 3.4 ns and position resolution of ≈ 50–145 μm. Charged particles that pass through the chamber ionize the gas mixture, and the resulting electron avalanche is captured by the anode wires, whereas the image charge is deposited onto the cathode strips. A coincidence of signals in multiple layers indicate the passage of the charged particle.

Figure 1 (right) shows a schematic layout of the on-chamber and off-chamber electronics. On each chamber, a set of Anode Front End Boards (AFEBs) perform the initial signal processing of the anode wire data, followed by a multi-layer coincidence identification in Anode Local Charged Track (ALCT) board. Cathode strip data is processed in the Cathode Front End Boards (CFEBs). A Low Voltage Distribution Board (LVDB) provides power to the on-chamber electronics. Electronics in the peripheral crates (off-chamber) further process the data for trigger and data acquisition (DAQ). The Trigger Motherboards (TMBs) combine ALCT and CFEB data into multi-layer coincidences

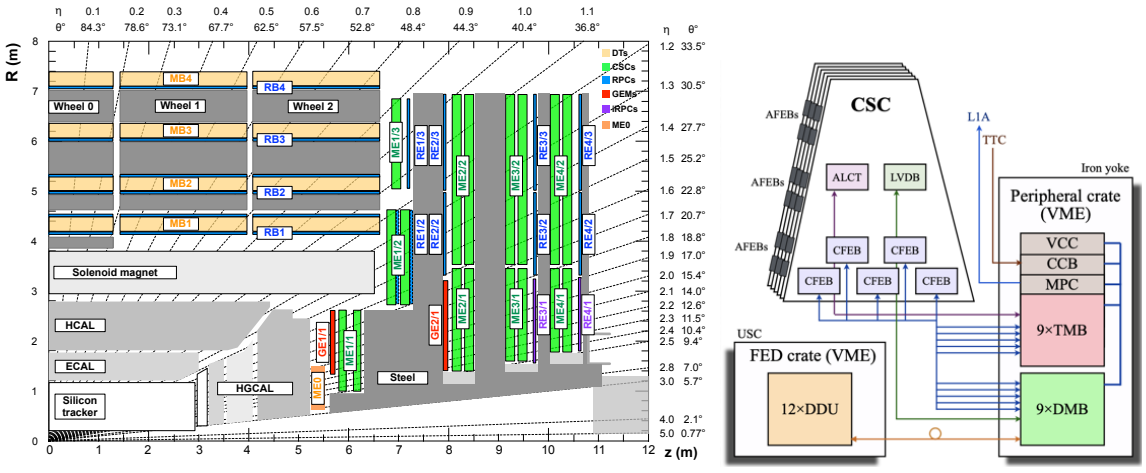

Figure 1: Left: Quadrant of the CMS detector in the Phase-2 configuration [2]. Drift Tubes (DTs) are shown in light orange, Cathode Strip Chambers (CSCs) in green, and Resistive Plate Chambers (RPCs) in blue. New GEM and RPC detectors are shown in red, dark orange, and purple. Right: Electronics layout of the CSC system [2].

suitable for triggering purposes. The Muon Port Card (MPC) receives trigger data from nine chambers and concentrates the data prior to sending it to the track-finders. Each CSC also has a Data Motherboard (DMB) that reads out the data and delivers it to a Detector Dependent Unit (DDU). The DDU is located in the Front End Driver crate and provides the interface between the CMS and CSC data acquisition systems. The remaining boards are the Voltage Crate Controller (VCC) and the Clock Control Board (CCB) which regulate the high-voltage for each gas gap and delivers the CMS clock respectively.

2. Upgrade of the CSC Electronics

The CERN LHC will be upgraded to the High-Luminosity LHC (HL-LHC) during the third long shutdown (LS3), from 2024 to 2027. The HL-LHC will have an instantaneous luminosity between $5 - 7.5 \times 10^{34}$ cm^{-2}s^{-1}, more than five times the design value. The HL-LHC is expected to deliver up to 3000 fb^{-1} of proton-proton collision data over ten years at a center-of-mass energy of $\sqrt{s}$ = 14 TeV . The CMS detector will have to be instrumented with new trigger and DAQ systems to handle the increasing data rate in the harsh radiation environment. Without upgrades the CSC system would experience data buffer overflows in CFEBs in the forward region, causing large inefficiencies in muon reconstruction [2]. In particular, CSCs in the ME2/1 station would experience a substantial loss of cathode data without upgrades. Additionally, the CSCs have severe memory limitations in the ALCT boards. Furthermore, the DMBs have insufficient bandwidth needed for the HL-LHC. Finally, components such as optical transceivers, memory units etc are not radiation-tolerant.

The CSC detectors will be upgraded during LS2 and LS3 to maintain their excellent muon detection capabilities. A three-fold upgrade program is underway. Firstly, nearly 1400 new electronics boards will be installed. Secondly, GEM trigger data from the GE1/1 and GE2/1 on-chamber electronics board will be sent to the ME1/1 and ME2/1 optical TMBs (OTMBs) respectively[1]. A third component involves the investigation of a new gas mixture with a smaller Global Warming Potential (GWP). The upgrade timeline is as follows. During LS2 (2019-2021), the system will undergo necessary on-detector refurbishments, i.e., the installation of new on-chamber electronics (DCFEB, ALCT, LVDB), new Optical TMBs (OTMBs), new high- and low-voltage services, and the GE1/1-ME1/1 optical link connection. These changes will ensure that during LS3 (2024-2027) only access to the peripheral racks is needed. New Optical DMBs (ODMBs) and DAQ backend board based on the Advanced Telecommunications Computing Architecture (ATCA) architecture will be installed. There are four workstreams spanning 2019-2020, with three completed before the outbreak of the COVID-19 pandemic, and one workstream which is expected to be completed by November 2020. We discuss below the upgrade of the electronics system and the ongoing gas-mixture and irradiation studies.

The ALCT boards are instrumented with Field Programmable Gate Arrays (FGPAs) mounted on the mezzanine board and based on Xilinx® Virtex-E chip. The current ALCT FPGAs have insufficient memory resources and output bandwidth and will therefore be replaced with FPGAs based on Spartan-6 with 9-12 more memory, 3-5 more logic resources, two times faster, see

[1]GE1/1 and GE2/1 refer to GEM chambers in station 1 and 2 respectively as shown in Fig. 1 (left). MEX/Y refers to CSCs in station X and ring Y.

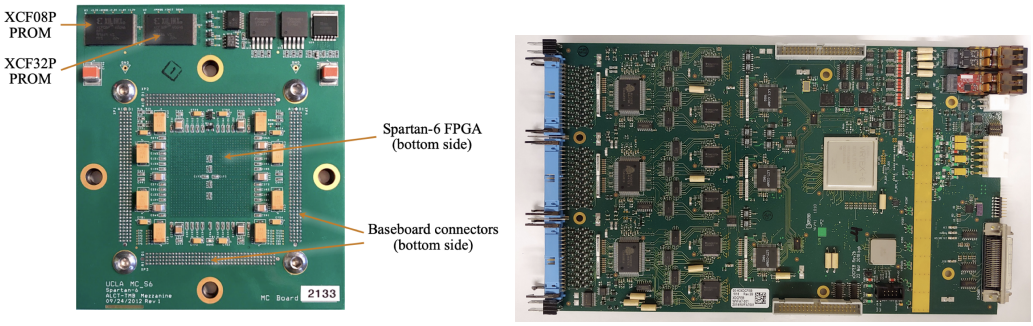

Figure 2: Left: ALCT mezzanine board. Right: An xDCFEB board. Reproduced from Ref. [2].

Fig. 2 (left). The CFEBs will be upgraded in the forward region. The original ME1/1 digital CFEBs (DCFEBs) will be replaced with radiation-tolerant xDCFEBs able to sustain up to ≈ 300 Gy, equivalent to three times the expected dose received after 10 years of HL-LHC operation. The chambers in the forward region covering ME2/1, ME3/1, and ME4/1 will have their CFEBs replaced with new digital versions, ME1/1 DCFEBs or similar. These DCFEBs have larger buffers, a fast 20 MHz flash analog-to-digital converter and are based on the Xilinx® Virtex-6 FPGA. New Low Voltage Distribution Boards (LVDBs) will be installed in the forward region and will provide more current for the ME1/1 xDCFEB, and more power for the ME2/1, ME3/1, and ME4/1 DCFEBs.

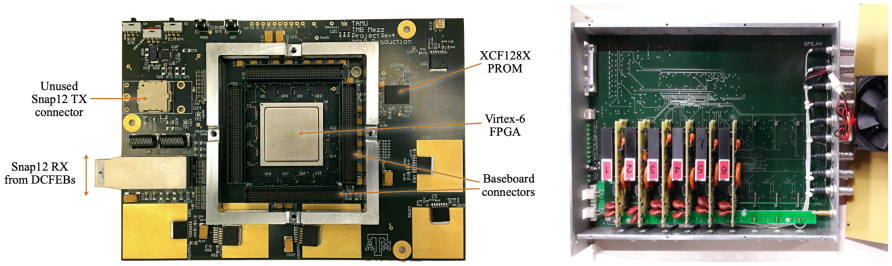

Figure 3: Left: OTMB mezzanine board with mounted Xilinx® Virtex-6 FPGA. Right: New High-Voltage Master Board. Reproduced from Ref. [2].

The forward chambers will also be instrumented with new motherboards. The current ME1/1 OTMBs will be replaced with faster, optical versions and will be connected with the nearby GE1/1 via optical fibers. Chambers in ME2/1, ME3/1 and ME4/1 will have faster optical versions of the TMB based on Xilinx® Virtex-6 FPGAs (Fig. 3 (left)). Finally, during LS2 the high-voltage system will be equipped with thirty-eight new 9-channel Master Boards that will absorb the dedicated ME1/1 CAEN® HV Master Boards. They also provide current measurements, and make it easier to operate and maintain the HV system. Figure 3 (right) shows the new Master Boards.

During LS3 the data motherboards (DMBs) of the forward chambers will be replaced with optical data motherboards (ODMBs). The existing ME1/1 ODMBs will be upgraded to ODMB7s, which will connect to the seven xDCFEBs in each ME1/1 CSC via a patch panel. The other forward chambers, ME2/1, ME3/1, and ME4/1 will receive ODMB5s. Both boards are based on the Xilinx® Kintex Ultrascale FPGA and have an output bandwidth up to 30 Gb/s. New ATCA-based boards will replace the current Front-End Driver (FED) boards and deliver data to the CSC DAQ system.

Improved muon trigger algorithms will be used to collect data on the HL-LHC [3]. Realistic simulations have shown that the current algorithms will lose efficiency in data taking conditions with 140 to 200 interactions per bunch crossing (pileup). ME1/1 in particular may lose up to 30% in efficiency without pileup mitigation in the OTMBs. New algorithms are being developed that produce CSC trigger primitives with high efficiency (> 95%), and higher position resolution ($\times 2-4$) and higher bending resolution ($\times 3$) than in Run-2. The ME1/1 and ME2/1 chambers will receive GEM primitives and will create integrated trigger primitives with an accurate measurement of the local muon bending angles GE1/1-ME1/1 and GE2/1-ME2/1. These improvements will increase the muon trigger efficiency and will decrease the rate. New solutions are also being developed to trigger on long-lived particles that decay into displaced muons or to hadronic showers in the endcap. Many of these Phase-2 improvements will be tested in the coming years, already during Run-3.

Figure 4: Left: Chamber extraction and reinstallation in the CMS underground cavern. Right: Refurbishment of the on-chamber electronics at SX5.

The CSC group has established a set of procedures to refurbish the on-chamber electronics during LS2 and this effort is well underway. Chambers are extracted from the underground cavern to the CSC laboratory at the surface level (SX5), see Fig. 4. On-chamber electronics boards are replaced and tested in a controlled environment in the CSC lab. Refurbished chambers are then returned to the cavern and re-installed onto the endcap disks in preparation for recommissioning. The COVID-19 crisis has had a serious impact on the schedule with in particular substantial delays and extensions of the work. Nevertheless, the LS2 work is on track to be completed by the end of 2020.

3. Irradiation and Gas Mixture Studies

As mentioned in Sec. 2 the HL-LHC will expose CSC electronic components to intense radiation, in particular on-board electronics in the inner-ring chambers. This requires radiation-tolerant optical transceivers, memory units etc. New components are being developed at participating institutes and are being tested with mixed hadron spectra at CHARM [4], with protons at the Texas A&M University (TAMU) Cyclotron Institute [5] and the University of California at Davis Crocker Nuclear Laboratory [6], and with neutrons and photons at the TAMU Nuclear Science Center TRIGA reactor [7]. During exposures of up to 300 Gy, the number of single-event upsets (bit-flips

caused by ionizing particles) and electronics dead-time is monitored. A recent test took place at the TAMU Cyclotron in June 2020 for the prototype erasable programmable read-only memory boards for inner-chamber ODMBs.

Finally, European regulations (No. 517/2014) restrict the usage of fluorinated greenhouse gases such as CF_4 which has a GWP $\approx$ 6500 for 100 years. CF_4 is one of the components in the CSC gas mixture (40% Ar, 50% CO_2, 10% CF_4) and serves as an anti-aging additive that prevents wire etching and polymerization. Alternative gas mixtures are being investigated at CERN with a 30×30 cm^2 prototype CSC. A two-fold approach is taken with longevity studies of gas mixtures with a smaller fraction of CF_4 and mixtures with a lower GWP, for instance HFO-1234ze (GWP < 1 for 100 years).

4. Summary

The CMS Cathode Strip Chamber system is being upgraded in preparation for the HL-LHC. The comprehensive upgrade program spans several years in LS2 (2019-2021) and LS3 (2024-2027). New radiation-tolerant electronics boards for trigger and data acquisition designed to operate at the HL-LHC will be installed. CSC detectors in the forward region will be connected to neighboring GEM detectors to produce integrated GEM-CSC trigger primitives. Algorithms are being designed to enhance the muon triggering capabilities and to expand the physics potential of CMS in Phase-2. Studies are also ongoing to replace high-GWP components in the CSC gas mixture. The LS2 portion of the upgrade is well underway and on track to be completed by the end of 2020.

Acknowledgements

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