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ATLAS ITk pixel detector overview

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For the HL-LHC upgrade the current ATLAS Inner Detector is replaced by an all-silicon system. The Pixel Detector will consist of 5 barrel layers and a number of rings, resulting in about 14 m^2 of instrumented area. Due to the huge non-ionizing fluence (over 2×10^{16} n_{eq}/cm^2) and ionizing dose (larger than 5 MGy), the two innermost layers, instrumented with 3D pixel sensors (L0) and 100 μm thin planar sensors (L1) will be replaced after about 5 years of operation. All hybrid detector modules will be read out by novel ASICs, implemented in 65 nm CMOS technology, with a bandwidth of up to 5 Gb/s. Data will be transmitted optically to the off-detector readout system. To save material in the servicing cables, serial powering is employed for low voltage. Large scale prototyping programmes are being carried out by all sub-systems. This paper will give an overview of the layout and current status of the development of the ITk Pixel Detector.

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1. Introduction

A High Luminosity upgrade of the Large Hadron Collider (LHC) at CERN, the HL-LHC, is planned to take place between 2025 and 2027. The new accelerator will deliver an instantaneous luminosity of 5 to $7.5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ and will allow to collect up to $4000\,\mathrm{fb^{-1}}$ of data over ten years of operations. About 140–200 proton–proton collisions per bunch crossing are expected at the site hosting the ATLAS experiment [1]. This dense particle environment is a challenge for the ATLAS detector [2] which will need to be upgraded to maintain and improve its performance. In particular, the whole Inner Detector will be replaced by a new full-silicon Inner Tracker (ITk).

2. The ATLAS ITk

The ITk consists of a strip detector and a pixel detector [3]. The former is composed four layers in the barrel starting at about 400 mm from the beam axis and six end-cap disks per side. The latter is made of five barrel layers from a radius of about 34 mm. In the forward region the pixel detector is completed by a novel and more flexible structure of concentric rings arranged at different radii. Due to the very large radiation doses expected over the full HL-LHC run period, the two innermost pixel barrel layers are designed to be replaceable and are foreseen to be exchanged after $2000\,\mathrm{fb^{-1}}$.

2.1 The pixel detector layout

The pixel detector is divided into an outer system, composed by three barrel layers (B4 to B2) with three corresponding groups of rings (R4 to R2), and an inner system with two barrel layers (B1 and B0) and three groups of rings: two in correspondence of the barrel layer radii (R1 and R0) and one in between the two (R0.5). Each ring is built out of two half-rings with a carbon core containing cooling and electrical services and can be positioned at a different distance along the beam line. The number of rings per layer and their position has been optimised to provide at least nine points per track and allows the extension of the pseudo-rapidity coverage up to $|\eta| = 4.0$.

2.2 Serial power and material budget

To minimise the impact of the material on the tracking performance, the whole ITk pixel detector uses carbon-based materials which have low mass, high stability and high thermal conductivity. The pixel modules are cooled with CO_2 through titanium tubes integrated into the carbon structures. A major contribution to the material budget in the present tracker is due to the electrical cabling. In the ITk pixel system its impact has been significantly reduced optimising the number of readout cables by using link sharing and a serial powering scheme to connect the pixel modules, minimising the service cable mass. The pixel modules use a Shunt-LDO regulator scheme to generate different supply voltages by parallel placed devices. This allows voltage regulation with a constant current from the external power source combining the feature of Low Drop-Out (LDO) regulators and shunt regulators. An average chain in the outer system is composed of about ten modules with several high voltage channels for serial powering chain to bias the sensors.

3. Pixel modules

The ITk pixel detectors are hybrid devices composed of one or more readout chips and a passive silicon sensor interconnected through a bump-bonding technique. These assemblies are then attached to a flexible Printed Circuit Board (PCB), called flex, to make a pixel module. The flex serves as interface to provide voltages and data connections for the chip as well as the reverse bias for the p-n junction of the sensors. Two kinds of pixel modules are foreseen for ITk: quad modules and triplets. The first are composed of single planar sensor readout by four chips and will instrument all layers and rings in the outer system as well as B1 and R1. The triplets consist instead of three single-chip 3D sensors connected to a common flex and will be employed in the innermost layer with two different designs to adapt to the geometry of the barrel and of the rings.

3.1 Front-end chip

The ITk chip is produced in 65 nm CMOS process and features a pixel size of $50 \times 50\,\mu m^2$. It has been derived from the RD53A prototype developed by the RD53 Collaboration at CERN for both the ATLAS and CMS experiments [4]. This prototype is only half size (approximately $1 \times 2\,cm^2$) and contains three different analog front end designs. One of these front ends, the differential front end, was chosen by the ATLAS Collaboration for the development of the ITkpix readout chip for ATLAS. The first version of this chip with the full-size reticle (approximately $2 \times 2\,cm^2$), the ITkpixV1, has been produced and it is now being characterised. The chip is specified to be radiation hard to more than 5 MGy with an in-time threshold of less than 1 ke. It is able to sustain a trigger rate of 1 MHz and a hit rate of up to $3\,GHz/cm^2$. With respect to the RD53A this new version of the chip also has an improved Shunt-LDO design for serial powering, data format including compression and command forwarding.

3.2 Sensor technologies

Different sensor technologies and pixel dimensions are used in the different layers of ITk. Silicon n-in-p planar pixel sensors with an active thickness of 150 µm are employed for the quad modules in the outer pixel system (B2-B4 and R2-R4), while the same planar sensor technology but with an active thickness of 100 µm instruments B1 and R1. Thin 3D silicon pixel sensors have been chosen for the innermost layer due to the outstanding radiation hardness of this technology. All planar pixel sensors will have a pixel size of $50 \times 50\,\mu m^2$ while 3D sensors with pixel cells of $25 \times 100\,\mu m^2$ will be employed in the flat barrel part (B0) and 3D sensors with pixel cells of $50 \times 50\,\mu m^2$ will be used in the innermost rings (R0 and R0.5).

Planar sensors. As opposite to the present n-in-n sensor technology employed in the current ATLAS pixel detector, the ITk uses n-in-p planar sensors which are produced with a single side approach. The single side process allows to ease the production by reducing the number of masking steps and consequently reduces the costs, which is especially relevant for the large area of the outer system. The active thickness has been chosen depending on the required radiation hardness to reduce the operational voltage necessary to optimise both hit efficiency and power dissipation.

In the outer layers the sensors will have to withstand an integrated particle fluence up to $2 \times 10^{15}\,n_{eq}/cm^2$ with a maximum power consumption of $10\,mW/cm^2$ calculated at the reference

temperature of −25 °C. Barrel and rings in the second innermost layer (B1 and R1) have instead more stringent constraints both in terms of radiation hardness, due to the proximity to the proton interaction point, and in terms of power dissipation, due to the limited space for the cooling pipes. In this case thinner sensors can achieve the required detection performance with a lower bias voltage even after large radiation doses to guarantee the required power consumption of less than 14 mW/cm^2 at −25 °C. Candidate 100 µm thick sensors for ITk demonstrated more than 97 % hit efficiency with a bias voltage of about 300 V after being exposed to a particle fluence of 5×10^{15} n_{eq}/cm^2 [5, 6].

Different biasing structures as well as the use of a temporary metal layer to define the quality of a sensor by measuring its electrical properties before interconnection to the readout chip have been studied. Some examples are shown in Figure 1.

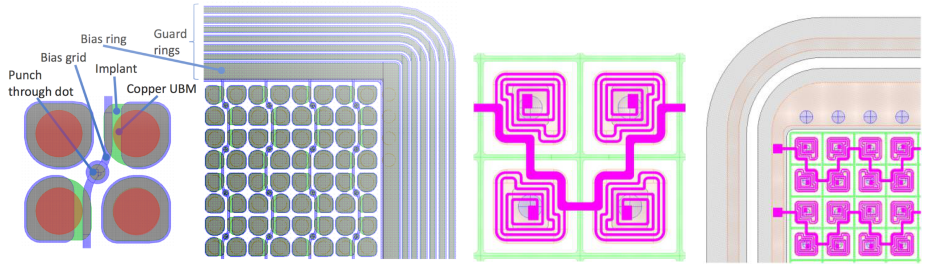

Figure 1: Examples of biasing structures employed in planar pixel sensor prototypes for ITk. On the left a new punch through structure design [6], on the right the bias resistor approach [7].

A punch-through method similar to the one used in the present planar pixel sensors has been investigated, but with a new geometry optimised to reduce the inefficiency after irradiation. This new design consists of bias dots shared by four adjacent pixels and connected by a wiggled metal line which overlaps as much as possible with the implants. After interconnection to the chip, the metal lines can be kept at ground potential or left floating. This second configuration has been demonstrated to improve the hit efficiency after irradiation.

An alternative biasing method consists of bias resistors on top of the pixel implants, also in this case connected with a wiggled metal line maximising the overlap with the implants. This design allows to improve the performance of the sensors in terms of hit efficiency after irradiation at the cost of a larger pixel capacitance and consequent noise which is not considered critical.

A third option is the use of a temporary metal layer deposited on the sensor to short the pixels at the wafer level. The metal layer is then removed before proceeding with the hybridisation process (UBM, thinning, dicing and flip-chipping). On the one hand, this method allows to measure the electrical characteristics of the sensors without introducing a permanent structure which alters the performance during operations. On the other hand, the sensors can be tested only at wafer level and the additional yield of the further processing needs to be consider in the production model.

Electrical and beam test results showed that all these sensor designs are compatible with the ITk specifications and can be used for the final production [5–7].

3D sensors. The 3D sensor technology has already been employed in the Insertable B-Layer (IBL) [8], the present innermost barrel layer of ATLAS. As opposite to the usual planar sensor design where the electrodes are implanted on the opposite surfaces of the active bulk, in 3D sensors

n-doped and p-doped column shaped electrodes are etched perpendicularly to the sensor surface. Thanks to this geometry, the charge collection distance is decoupled from the active thickness. This allows to improve the radiation hardness by reducing the electrode distance without decreasing the amount of charge created by a crossing Minimum Ionising Particle (MIP).

With respect to the IBL design, the ITk 3D pixel sensors feature smaller pixel cells ($25 \times 100\,\mu m^2$ in the barrel and $50 \times 50\,\mu m^2$ in the rings instead of the $50 \times 250\,\mu m^2$ of IBL) and a thinner active substrate (150 µm instead of 250 µm). The different 3D pixel designs are shown in Figure 2. For both cell dimensions of ITk, the pixel is defined by one n-doped column surrounded by four p-doped columns. The smaller dimension of the pixels translates directly into an improved radiation hardness due to the proximity of the columns which reduces the charge-trapping probability after irradiation. Moreover, the thinner active bulk reduces the occupancy for particles crossing the sensors at an angle with respect to the surface.

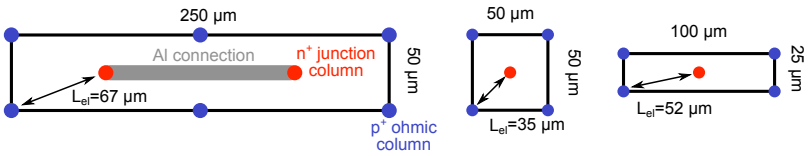

Figure 2: Different 3D pixel designs [9]. From left to right: the pixel cell of the 3D pixel sensors employed in IBL; $50 \times 50\,\mu m^2$ and $25 \times 100\,\mu m^2$ pixel cells for the ITk innermost barrel layer and rings, respectively

To achieve thinner active substrates, the fabrication process has been modified with respect to the IBL double-sided approach to be compatible with Silicon on Silicon wafers, which consist of a high-resistivity Float Zone active silicon layer directly bonded to a low-resistivity Czochralsky silicon handle wafer. A so-called single-side approach is employed which consists of etching both p-type and n-type columns from the front side. The readout columns (n-type) stop at a safety distance of ~25 µm from the handle wafer to avoid early breakdown, while the p-type columns are etched into the handle wafer. The handle wafer is then thinned down and a metal layer is deposited to supply the bias voltage from the backside. As for the IBL sensors the active bulk of the ITk 3D sensors is made of p-type silicon. Both $50 \times 50\,\mu m^2$ and $25 \times 100\,\mu m^2$ sensor pixel designs are compatible with the ITkpix chip layout thanks to a proper routing of the readout columns to the bump bonding pads.

These novel 3D sensors developed for ITk and coupled to the RD53A prototype chip have demonstrated outstanding radiation hardness up to a particle fluence of $10^{16}\,n_{eq}/cm^2$ by achieving more than 97 % hit efficiency with a bias voltage lower than 100 V and a power dissipation lower than $10\,mW/cm^2$ at −25 °C as required for the ITk specifications of the innermost layer and rings [9].

4. Data transmission

Due to the high radiation levels expected inside the detector the data transmission links will be split into an electrical part bringing the signal from the modules to an end-plate region with opto-components, and an optical part taking the data out of the detector. A 5 Gbps readout data rate is required to fully exploit the performance of the new front-end chip. The data is read out at 1.28 Gbps with up to four links per chip and is driven through twin-axial cables up to an opto-board consisting of a Gigabit receiver chip (GCBR), a low-power Gigabit Transceiver (lpGBT)

and an optical link module for aggregation and electro-optical conversion. The optical signals are then output at more than 5.12 Gbps from the opto-board to reach the external readout system. A system test development with all elements has been put in place which achieved the required performance [10].

5. Conclusions

The ITk layout of the pixel detector for the ATLAS Phase-II at the HL-LHC has been finalised as well as the choice of the sensor technologies consisting of 150 µm and 100 µm thick n-in-p planar pixel sensors and 3D sensors with small pixel cells. Moreover, the first version of the new full-size ITk readout chip has been developed and produced, and it is presently being characterised. Key features of the new detector are the use of serial powering for the modules and cooling through CO_2 which allow to significantly reduce the impact of the material on the tracking performance. Several demonstrator programmes are presently ongoing involving all sub-systems with thermal and electrical prototypes including also serial powering chains. The ITk project is moving from design to prototyping and the pre-production of many components is about to start.

References

[1] G. Apollinari, I. Béjar Alonso, O. Brüning, P. Fessia, M. Lamont, L. Rossi, L. Tavian, *High-Luminosity Large Hadron Collider (HL-LHC): Technical Design Report V. 0.1*, (2017) CERN-2017-007-M.

[2] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* **3** (2008), S08003.

[3] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, (2017) CERN-LHCC-2017-021, ATLAS-TDR-030.

[4] RD53 Collaboration, *The RD53A Integrated Circuit*, (2017) CERN-RD53-PUB-17-001.

[5] G. Calderini et al., *Performance of the FBK/INFN/LPNHE thin active edge pixel detectors for the upgrade of the ATLAS Inner Tracker*, *JINST* **14** (2019) 07, C07001.

[6] J. Beyer, *Optimisation of pixel modules for the ATLAS inner tracker at the high-luminosity LHC*, (2019) PhD thesis, LMU Munich.

[7] K. Nakamura et al., *Development of a radiation tolerant fine pitch planar pixel detector by HPK/KEK*, *Nucl. Instrum. Meth. A* **924** (2019) 64-68.

[8] B. Abbot et al., *Production and integration of the ATLAS Insertable B-Layer*, *JINST* **13** (2018) T05008.

[9] S. Terzo et al., *A new generation of radiation hard 3D pixel sensors for the ATLAS upgrade*, *Nucl. Instrum. Meth. A* **982** (2020) 164587.

[10] C. Chen et al., *1.28 and 5.12 Gbps multi-channel twinax cable receiver ASICs for the ATLAS Inner Tracker Pixel Detector upgrade*, *Nucl. Instrum. Meth. A* **981** (2020) 164439.