A muon tracking algorithm for the Level 1 trigger in the CMS barrel muon chambers during HL-LHC

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The electronics of the Compact Muon Solenoid (CMS) Drift Tube (DT) chambers will need to be replaced for the High Luminosity LHC (HL-LHC) operation, also called Phase 2, due to the increase of occupancy and trigger rates in the detector, which cannot be sustained by the present system. New electronics are being designed that will forward asynchronously the totality of the chamber signals to the counting room, at full resolution. The new back-end system will be in charge of building the trigger primitives (TP) of each chamber out of this asynchronous information, aiming at achieving resolutions comparable to the ones of the offline reconstruction. The new improved functionality will help to improve the resilience to potential ageing situations. An algorithm for the TP generation that will run in this new back-end system has been developed and implemented in firmware. The performance of this algorithm has been validated through different methods: from a software emulation approach to hardware implementation tests. The performance obtained is very good, with optimal timing and position resolutions, close to the ultimate performance of the DT chambers. One important validation step was including the implementation of this algorithm in a prototype chain of the HL-LHC electronics, which has been operated with real DT chambers during cosmic data taking. The new TP generation has been implemented in the so-called AB7, spare uTCA boards from the present DT system which host Xilinx Virtex 7 FPGAs. The performance of this prototyping system has been verified and will be presented in this contribution, showing the feasibility of the design for the expected functionality during HL-LHC.

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CMS is one of the two general purpose detectors at the LHC. It has been designed with a two-level trigger system: the Level 1 trigger (L1) and the High Level Trigger (HLT). Muon trigger and reconstruction are provided by the DT chambers in the barrel and the cathode strip chambers (CSC) in the endcap, both complemented by a system of resistive plate chambers (RPC). The basic element of the DT detector is the drift cell. Four staggered layers of parallel cells form a superlayer (SL). A chamber is composed by two superlayers measuring the $r - \phi$ coordinates, and an orthogonal superlayer measuring the r-z coordinates. A more detailed description of the CMS detector and the CMS DT chambers can be found in [1] and [2] respectively. For Phase 2 the full DT electronics will be replaced and TP algorithms will be implemented in powerful FPGAs, resulting in a substantial improvement of the physics performance.

The **Analytical Method** is an algorithm for TP generation in the DT chambers in HL-LHC. It profits from the better electronics time binning in Phase 2 (1 ns instead of 12.5 ns at present). The algorithm is capable of computing a TP's crossing time, both in ns (t_0) and bunch crossing (BX) units, together with muon track position and local direction. The inputs to this algorithm are the time and cell number of all signals detected in a superlayer and can be described in three steps: grouping of hits, muon track fitting in a given SL and correlation between SLs in a chamber. After building the AM DT primitives and clustering the RPC hits, the information from both subdetectors can be combined.
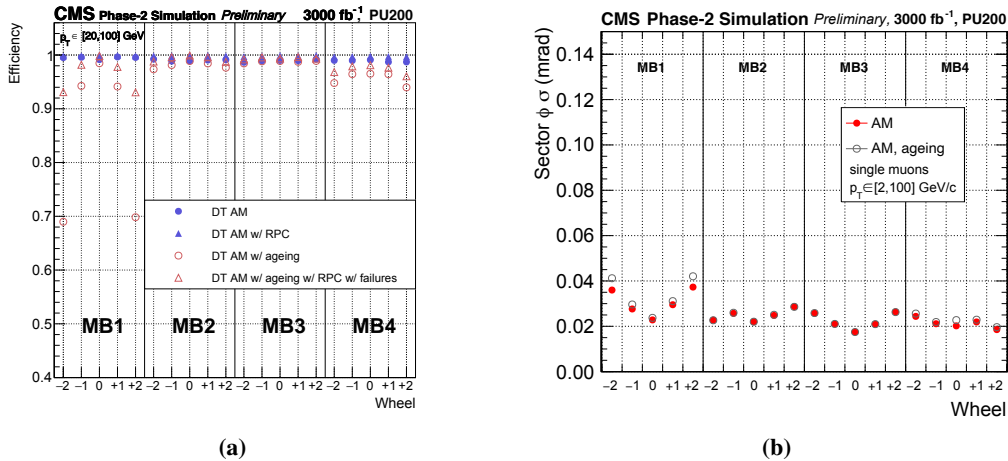

Figure 1: (a) Barrel Muon Phase 2 TP efficiency in the good BX with respect to offline segments matched with a generated muon and (b) position (*sector phi*) core resolution with respect to the simulated hits in the muon chambers. Both figures show results with and without the ageing scenario. See [3].

The algorithm's performance has been evaluated in a 200 average pile-up simulated sample produced for the L1 Trigger Phase 2 Upgrade TDR [3]. Figure 1 (a) shows the DT-only efficiency is in general very high except for some drops related to regions very affected by the DT ageing. The inclusion of RPC improves efficiency in these most affected regions. Figure 1 (b) shows that *sector* ϕ resolution (position in global coordinates) is < 0.05 mrad for every chamber, improving a factor ~ 6 with respect to the Phase 1 TPs.

The AM has been implemented in VHDL code in order to estimate its performance in real time conditions inside prototyping FPGAs. Tests of firmware-emulator comparison have been performed

in a dedicated test stand at CIEMAT injecting DT hits from all chambers in the CMS detector. Using these hits, AM firmware generates the TPs, which can be then compared to the ones obtained by the software emulator. Figure 2 (a) shows the level of agreement in BX when comparing the primitives obtained by the firmware and the emulator with the same hits and lateralities. The insert shows an agreement in the fitted time value at the level of Least Significant Bit (1 ns). This agreement is also reached in fitted position and local direction.
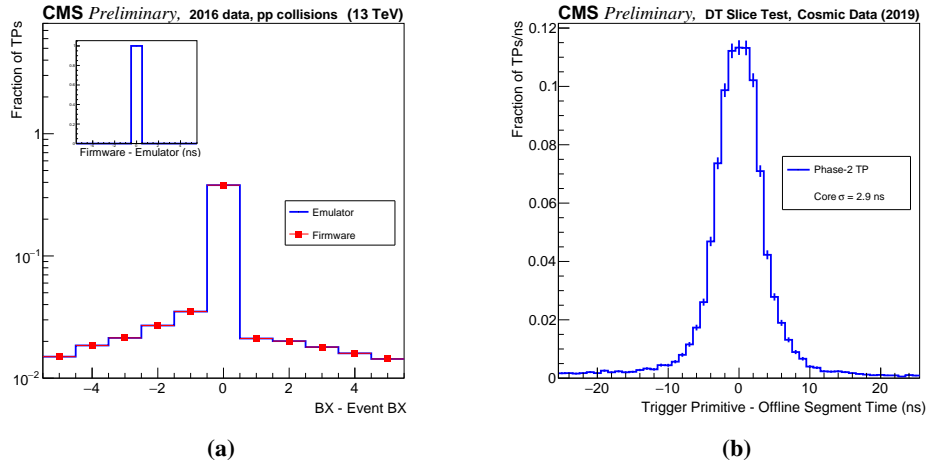

(a)

(b)

Figure 2: (a) Difference in BX assignment between emulator primitives and event BX (blue) and firmware primitives and event BX (red) and (b) difference between the crossing time of incoming cosmic muons computed by the DT offline reconstruction and the Phase 2 AM DT local trigger in the Slice Test set-up. See [3].

During the Long Shutdown 2 a complete exercise was made to instrument one sector (wheel +2 sector 12) of the CMS detector with the HL-LHC DT electronics front-end and back-end prototypes, the so-called DT Slice Test. This way, both Phase 1 and Phase 2 electronics can be run in real conditions inside the CMS infrastructure. One of these back-end boards (the so-called AB7) runs the AM firmware, so it can be validated using real cosmic muons. Figure 2 (b) shows the difference between the crossing time of incoming cosmic muons computed by the DT offline reconstruction and the primitives obtained by the Analytical Method firmware. The core resolution of this distribution is of few ns, while for the Phase 1 system the trigger output time is given in BX units (25 ns step).

References

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