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Enabling low-power MAPS-based space trackers: a sparsified readout based on smart clock gating for the High Energy Particle Detector HEPD-02

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The adoption of pixel sensors for space-based tracking detectors requires low power consumption and enhanced heat dissipation to cope with the satellite power and cooling constraints. The High Energy Particle Detector (HEPD) tracker onboard the CSES-02 will be the first application of monolithic active pixel sensors (MAPS) to a satellite-based experiment. This result is achieved with a parallel sparsified readout architecture implemented on a single low-power FPGA chip, which manages the 150 ALPIDE chips of the three-plane tracker. The power consumption is reduced by reading out the ALPIDE chips via the control line instead of the high speed data link, and by distributing the clock only to the portions of the detector crossed by a particle. The readout concept presented in this contribution allows to deal with both the required performance and the power constraints, and is scalable to larger and more complex detectors.

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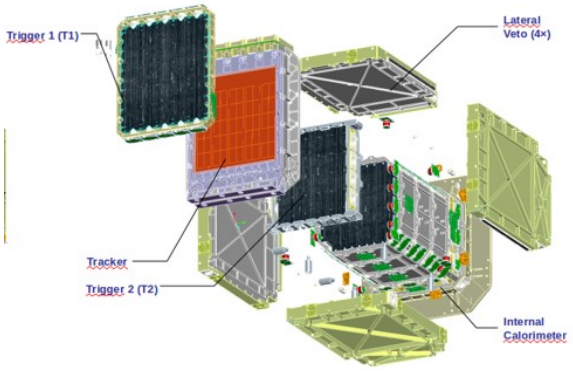

Figure 1: Exploded view of the HEPD-02 apparatus. The assembled dimensions are approximately 20 × 20 × 40 cm^3. The tracker follows the first trigger scintillator layer (T1).

1. Introduction: HEPD-02

The High-Energy Particle Detector HEPD-02[1] is one of the payloads that will equip the China Seismo Electromagnetic Satellite (CSES-02)[2] to be launched by the end of 2022.

The CSES space mission is dedicated to the monitoring of variations in the electromagnetic fields and waves, plasma parameters and particle fluxes, induced by natural sources and artificial emitters in the near-Earth space, investigating possible correlations between such perturbations and the occurrence of high-magnitude seismic events. Other fundamental targets are the study of space-weather phenomena and cosmic-ray propagation.

HEPD-02 (Figure 1) is being currently developed by the Italian Limadou Collaboration. It is aimed at measuring the flux of charged particles trapped in the terrestrial magnetosphere; it comprises various layers of scintillator detectors and a tracker, optimized for detection of individual electrons and protons with kinetic energies in the range from 3 to 100 MeV and from 30 to 200 MeV, respectively, with identification of particle species (proton, electron, nucleus) and measurement of energy and incoming direction, specifically with angular resolution better than 10° for electrons.

2. HEPD-02 tracker

The HEPD-02 tracker (Figure 2) is composed of 5 adjacent turrets, each made of 3 planes or "staves" with active area 15 x 3 cm^2 each. A stave (Figure 3) houses two rows of 5 ALPIDE[3] monolithic active pixel sensors (MAPS) for a total of 150 ALPIDE sensors (80 Mpixels).

On each stave, the 10 ALPIDE chips are positioned and glued on a CFRP[1] mechanical support and covered by a custom-designed FPC (Flexible Printed Circuit) made by kapton insulator and copper tracks, connected to the chips via triple-redundancy bondings, for signal and power routing. A custom-designed TSP (Tracker SPlitter) compact PCB is positioned on the turret side for cabled interface with power and control/readout electronics. The FPC/TSP connection is made via soldered wires (few cm length).

[1]Carbon-fiber-reinforced polymer.

Figure 2: The HEPD-02 tracker design.

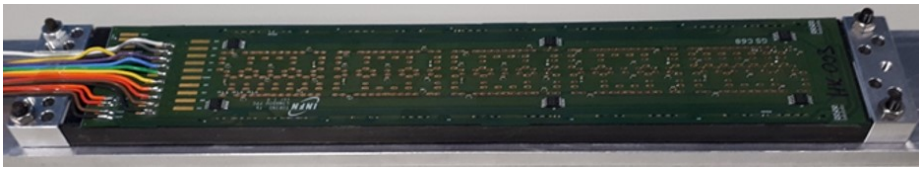

Figure 3: A tracker stave: the FPC and soldered wirings toward TSP are clearly visible.

3. ALPIDE MAPS in space

The ALPIDE chip, developed by the ALICE collaboration for the Inner Tracker System Upgrade at LHC (CERN), is made of 512×1024 pixels with 27 mm $\times$ 29 mm pitch on an area of 15×30 mm^2. The ALPIDE chip (Figure 4) employed in HEPD-02 is fabricated on a 50 μm thick Si substrate. The pixel structure is shown in Figure 5; the charge is collected by diffusion, with an applied back-bias up to -6 V and a noise of only $\sim$ 10 *e*/pixel. The pixel integrates a threshold readout circuit in 180 nm CMOS technology; this analog front-end circuit gives binary zero-suppressed output. The ALPIDE chip contains an overall readout and control digital circuit which implements a sparsified readout with data from only the hit pixels.

The use of ALPIDE in HEPD-02 constitutes the first space application of MAPS. Compared to the traditional hybrid microstrip sensors employed in previous space experiments, MAPS enable higher granularity, low noise, compact assembly (with sensor and front-end circuit on the same Si substrate) with much fewer bonding interconnections, binary pixel readout avoiding the need for external digitization circuitry, excellent spacial resolution (5 μm for Z=1 MIP); last but not least, production costs are lower.

Since the MAPS technology has not been designed for use in space, several challenges have been faced in the design of the HEPD-02 tracker, namely to provide adequate assembly stiffness in view of the mechanical stresses foreseen at launch, resistance to repeated thermal cycling in vacuum, low enough power consumption to fit in the requirements for the satellite application; this last aspect is the object of the current report and will be discussed below.

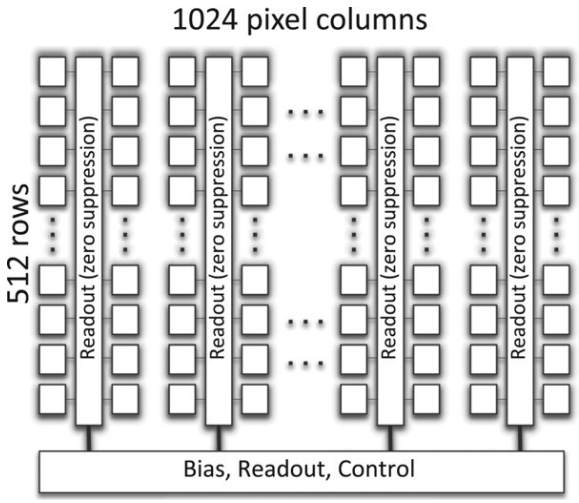

Figure 4: The ALPIDE internal structure.

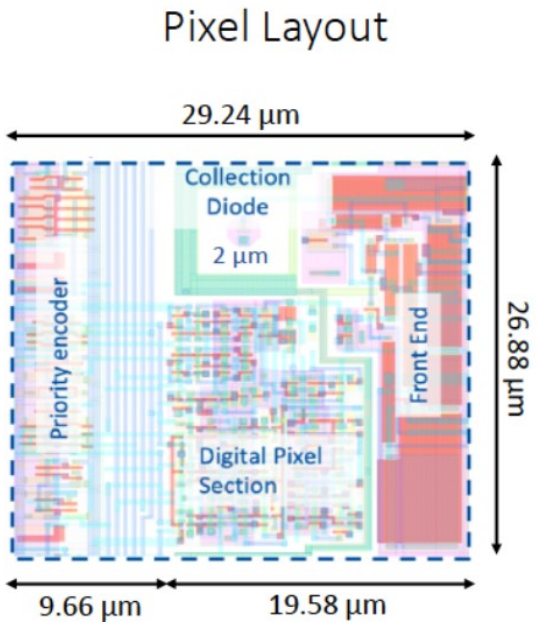

Figure 5: Structure of the ALPIDE pixel.

4. Low-power readout architecture

The satellite application imposes a strong design optimization effort in terms of power, to match the budget constraints (~16 W available for the whole tracker, including the readout electronics) and to allow for an adequate cooling in vacuum (with no air convection) by pure conduction through the stave CFRP toward the external Al-alloy frame. An application-specific low-power parallel readout architecture (Figure 6) has been therefore implemented, by introducing several changes with respect to the one originally designed for ALICE detector at CERN. The most interesting features are explained in what follows.

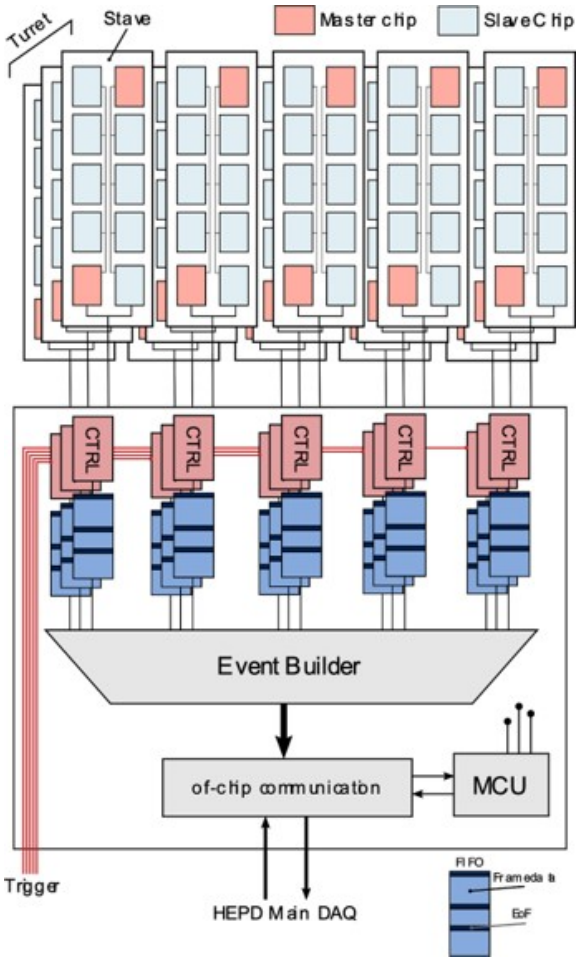

Figure 6: Structure of the tracker readout.

- ALPIDE master-slave architecture. Each stave contains two chains of 5 chips with one master each. The readout of the 4 ALPIDE slaves is made by the master through a local 80 Mbps bus.
- ALPIDE master readout through serial slow-control line (up to 40 Mbps). The ALPIDE built-in fast data transmission unit (DTU, 1.2 Gpbs) is kept permanently switched-off; the external readout is implemented via the slow-control line instead.

With such configuration, the maximum power consumption for each ALPIDE chip amounts to 55 mW (to be compared with up to 150 mW foreseen in the application at CERN). Correspondingly, the dead time is increased but still acceptable for the HEPD-02 application, given the relatively low trigger rate sustainable by the system as a whole (up to few kHz, varying along the orbit).

- Minimal external control and readout electronics. The whole tracker control and readout is managed by a single fully customized board (TDAQ) interfacing with the central unit of the HEPD-02 system and implementing only the necessary functionalities to fully assure the required tracker operation and performance. The TDAQ board contains a single Xilinx

Artix 7 FPGA with auxiliary flash EEPROM and SRAM memories, with a maximum power consumption matching the 3 W allowable budget. Up to 15 dedicated logic modules (one per stave) can be simultaneously activated to handle the full ALPIDE housekeeping and data acquisition. Calibration (threshold setting, exclusions of dead/noisy pixels etc.) and service procedure are implemented in a Microblaze soft processor structure inside the FPGA.

- Clock gating: ALPIDE clock is normally kept off, set on only as a response to a particle trigger from the HEPD-02 scintillator system and only for the time necessary for event readout.
- Dynamic scaling of clock frequency: the clock frequency can be dynamically reduced in regions of the orbit where the trigger rate is significantly lower (i.e. when the satellite is out of the Van Allen belts) and an increase of data readout dead time is therefore acceptable.
- Segmentation of the first HEPD-02 trigger plane in 5 bars, each one set on top of a tracker turret. This allows to distribute the clock signal only to the turret below the activated trigger bar and to the adjacent ones, thus avoiding the readout of other turrets not directly involved in the event.

5. Conclusions

In this work we presented the optimized low-power readout architecture developed for employment of a MAPS-based tracker in the HEPD-02 apparatus. This is the first ever space application of MAPS: while several advantages are given by MAPS with respect to traditional hybrid microstrip sensors, a strong design effort has been necessary to reduce the power consumption in such a way to match the tight requirements given by the satellite mission.

References

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