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KM3NeT Acquisition Electronics: New Developments and Advances in Reliability

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The KM3NeT Collaboration is currently building a neutrino observatory at the bottom of the Mediterranean Sea. The telescopes are equipped with thousands of Digital Optical Modules hosted in glass spheres, instrumenting a volume of several cubic kilometers. The acquisition electronics is housed inside the glass sphere performing the readout of the 31 Photo Multiplier Tubes of the Digital Optical Module. This work presents the latest developments in the acquisition electronics including the increase in efficiency on the Power Board, the new developments on the Central Logic Board and the different reliability methods used in KM3NeT to make the acquisition electronics more reliable.

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1. KM3NeT Introduction

KM3NeT [1] is a large infrastructure currently under construction with already six Detection Units (DU) installed in the Italian site (ARCA) [2], and six DUs in the French site (ORCA) [3]. The telescopes are designed to detect the Cherenkov photons emitted by relativistic charged particles produced in neutrino interactions around the detector. A 17-inch diameter pressure-resistant glass sphere housing 31 3-inch PMTs together with the front-end and readout electronics [4, 5] constitutes a DOM [6, 7]. A DU is composed of eighteen DOMs, mounted in a vertical structure. The DUs are anchored to the seabed and are keep vertical due to the flotation of the DOM and to a buoy on top of the DU. A matrix of DOMs detects the Cherenkov photons and from the data obtained, it is possible to reconstruct the trajectory and energy of the neutrino.

When a photon impinges on the PMT cathode, and depending on the quantum efficiency (usually $\sim$ 30%), an electron avalanche is produced in the PMT. If the PMT electrical signal surpasses the threshold of a discriminator, it generates a LVDS signal. The time duration of the signal is called ToT. The PMT base contains the electronics of the discriminator as well as those for the generation of the High Voltage that supplies the PMT. All LVDS signals are routed by a SCB to the CLB. The readout acquisition of the PMT data is performed in the CLB.

The readout firmware runs on a 160T Kintex-7 FPGA [8]. The firmware modules are configured and controlled by an embedded LM32 micro-processor. 31 TDC channels are implemented in the FPGA. They digitize the LVDS signals to obtain both the arrival time of the pulse and its ToT. The PMT signal digitized by the TDC is called a "hit". Once a hit is obtained, a State Machine organizes the hits generated by the TDC and encodes these into UDP Jumbo frames to be sent to the shore station via the CLB optical link. All the readout information is sent to the shore station without any data filtering. The readout is organized and sent in time intervals of 100 ms, called a "time slice". In order to combine and analyze the data provided by all the DOMs, the White Rabbit protocol [9] is used to synchronize the clocks of all the CLBs of the detector with 1 ns resolution. A power board housed in the DOM converts the input 12 V into the different voltages needed by the DOM electronics.

2. DOM Electronics Improvements

A new version of the CLB and the PB has been developed taking into account the return of experience from the manufacturing of electronics boards for 31 DU, twelve of which have already been deployed and are taking data. The redesign have focused on functionality, reliability and efficiency improvements.

2.1 Central Logic Board Version 4

The improvements in the main acquisition electronics boards involve the adjustment of the mechanics coupling with the rest of the DOM components; the addition of extra sensors, such as a pressure sensor; the addition of the compass and tilt sensors directly on the CLB PCB instead of in a daughter board; the addition of an additional flash memory in order to increase the overall operation life of the flash memories; the improvement of the oscillator system in order to reduce the phase noise of the CLB clocks, improving the synchronization levels of the detector; the replacement of

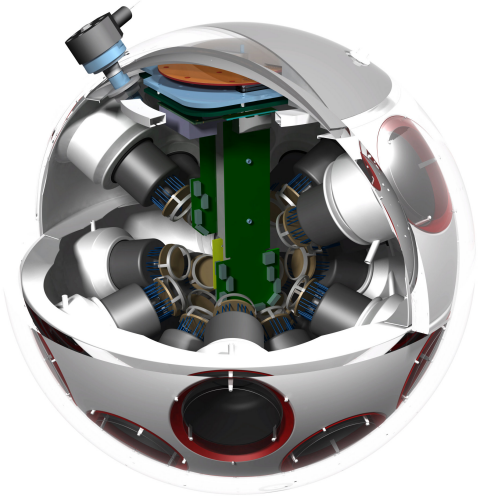

Figure 1: Open view of a DOM.

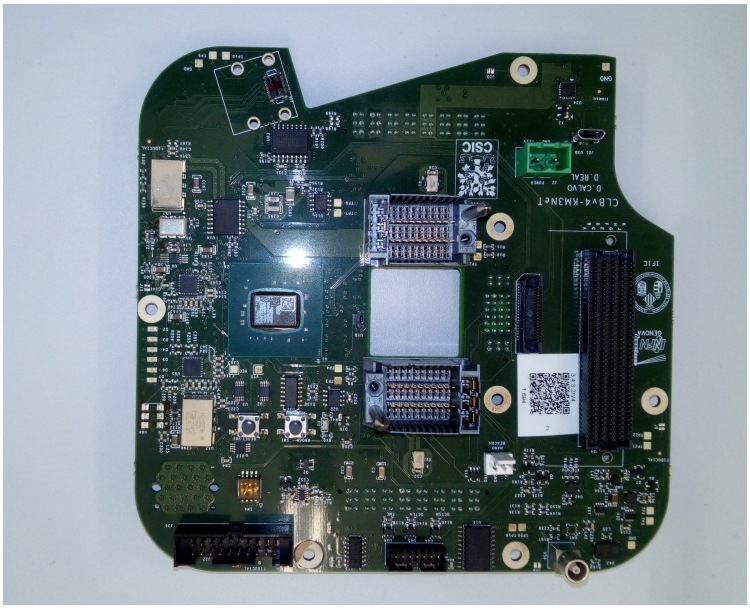

Figure 2: Pre-series CLBv4.

the optical transceiver with a higher reliability model; and a hardware watchdog to protect the CLB from losing access due to reconfiguration errors.

2.1.1 Clock Generation System

The CLBv4 incorporates two different clock generator systems. The first system is identical to the system used in the previous version of the board. A clock of 25 MHz generated in a quartz oscillator is used by a Digital Clock Manager (DCM) to increase the frequency to 125 MHz. The 124.992 MHz is synthesized similarly. Both frequencies are used by White Rabbit to measure the phase using the Dual Mixer Time Difference (DMTD) technique.

Table 1: DOM Voltages, currents and efficiency of the PB broken down by power rail. The efficiencies of the previous version of PB are given as well for comparison.

Volt (V)	Current(A)	Efficiency PB v2.3 (%)	Efficiency PB v3.0 (%)
1	0.13	80	80
1.8	0.33	80	80
2.5	0.33	60	78
3.3	0.81	65	90
3.3 PMTs	0.46	90	90
5	0.10	60	90

The novelty in the CLBv4 is the system generating the frequencies needed by White Rabbit directly from quartz oscillators manufactured to oscillate precisely at the required frequencies. As the frequency is directly generated, the quality of the clock signal improves, and so does the synchronization quality achieved by the CLBv4.

In a first step, four CLBv4 prototypes have been produced. A CLBv4 has been connected to a standard WR switch in order to test the synchronization stability. The PPS skew has been measured, showing a low jitter (values below ± 25 ps standard deviation). Before measuring the skew, the CLBv4 is switched off/on, to simulate the worst conditions related to synchronization and when the worst values of jitter are obtained.

2.2 Power Board version 4

The PB improvements include a modification the DC/DC converters to operate the PB more efficiently. The efficiency increase results in decreasing the power consumption, thermal losses and the temperature inside the DOM, which redounds in an increase of the electronics reliability.

PBv4 replace some DC/DC converters to have better efficiency. In particular, the DC/DC converters of the rails of 2.5 V, 3.3 V and 5 V have been changed, obtaining an overall decrease of 1 Watt with a significant efficiency improvement with respect to the previous version of PB. (See Table 1)

3. Reliability: FIDES HALT

3.1 Reliability

The reliability of the PBs and CLBs have been evaluated. The FIDES analysis has been performed and compared with the previous version of the boards.

In addition, in order to assess the reliability of the boards, both boards have undergone the Highly Accelerated Life Test (HALT) procedure. The goal in KM3NeT is to increase the reliability of the boards in an early state of the developing process.

3.2 FIDES

is used by KM3NeT to assess the reliability of the electronics boards [4, 10].FIDES is one of the most updated methods, being this the reason for their use in KM3NeT.

In order to assess the reliability of the electronics boards[4, 10], KM3NeT is using FIDES [11], one of the most updated methods.

A handbook predicting the reliability of the components is provided by FIDES, as well as a guide for auditing the manufacturing process. With this method, it is possible to compute an estimate of the Failure In Time (FIT, given in failures in 10^9 hours) or Mean Time Between Failure (MTBF) of the board analyzed. The FIDES method takes into account the operation condition or stress expected during operation, the life profile and the technological factors that affect the board reliability. In addition to the estimated FIT, the method can signal weak points in the design of the board in a very preliminary stage, saving time and money in the process to develop the electronics boards.

The PB FIT value has decreased to 783, while the FIT of the previous version of the PB was 947. The FIT of the CLBv4 is slightly higher than in version 2, 416 versus 404, but in the CLBv4 there are additional components and includes the compass and tiltmeter components which, before, were outside the CLB.

3.3 HALT

HALT is an experimental method to assess the reliability of a board by applying various forms of stress. It is applied only to a reduced number of boards, usually 4 to 6, at an early design stage.

In KM3NeT, we implemented thermal extremes and extreme rates of change, and recommended vibration and the combination of thermal and vibration. During HALT testing, it is essential to operate the product and to ensure its functionality. Test setups should be optimized to maximize the functional test coverage. The test setup should also allow for remote operation of the test from outside the environmental chamber. The next subsections describe the HALT processes applied in KM3NeT to the CLB and the PB.

3.3.1 Temperature Step Stress Tests

The procedure for the Temperature Step Stress is defined with the following steps:

- The device is inserted in the climatic chamber, and it is powered on
- The power consumption is measured
- The correct behavior of the device is checked
- Starting at ambient temperature (i.e. 25 °C), decrements of 5 °C per step are applied
- Wait 10 minutes for the temperature to stabilize
- After each step, the behavior of the board is checked
- Before going to the next step, the board is switched off/on
- The behavior of the board is checked again
- Continue decreasing the temperature until failure or the lowest temperature achievable by the climatic chamber is reached

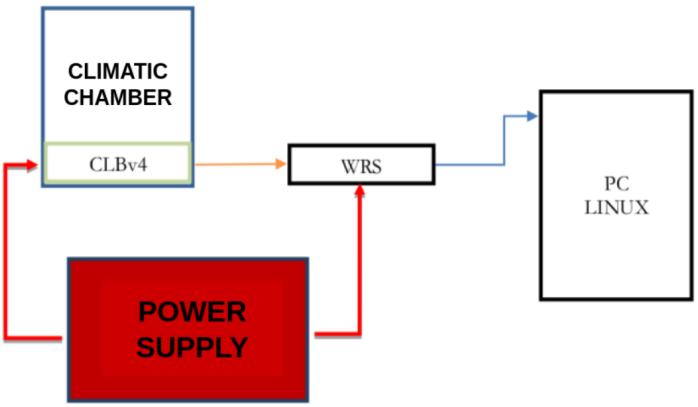

Figure 3: System configuration for the HALT tests.

- If possible, the failure should be fixed and one should continue to decrease the temperature
- The same procedure should be then performed with increasing temperature.

3.3.2 Extreme Temperature Stress Tests

Once the Temperature Step Stress is completed, Extreme Temperature Stress tests are carried out. From ambient temperature, the temperature is decreased to the minimum of the chamber at the maximum pace allowed by the chamber. In our case, this corresponds to -40 °C with a pace of 1 °C per minute. The temperature is left to stabilize for at least 15 minutes at -40 °C, then functional tests are performed to check the communication of the boards under tests. The next step is to power cycle the board and to perform the functional tests again. If everything is correct, then the chamber should go to the maximum temperature, in this case 110 °C with a pace of 1 °C per minute. At 110 °C, the temperature is left to stabilize for 15 minutes and the functional test is performed again. If the test is successful, the system should be rebooted and the functional test should be performed for the last time.

3.4 HALT implementation in the KM3NeT

The CLBs and PBs have been tested in a climatic chamber, ranging from -40 °C to 110 °C. The CLB did not use any kind of thermal dissipation structure. The CLB, together with the associated PB under test is inside the climatic chamber, connected with an external WRS outside the climatic chamber. The WWRS is connected to an external Personal Computer (PC), from where it is possible to communicate with the CLB and to check if the CLB is synchronized.

The functional tests consist in checking the communication from the PC to the CLB via the WRS, monitoring the synchronization of the CLB, and the UDP data transmission from the CLB, logging the temperatures. The firmware image has been updated, including a reboot, every 5 °C to check the reconfiguration process. The temperature of the FPGA is monitored as well as the power consumption of the CLBv4.

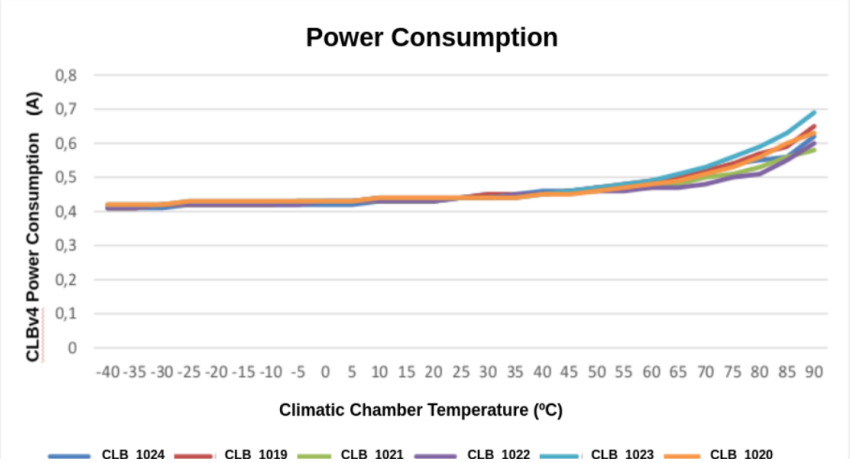

Figure 4: Power consumption of the system during the HALT tests.

3.5 HALT results for the CLBv4 and the PBv4

In total, six CLBv4 and PBv4 were tested. The five boards work fine in the range -40 °C to 95 °C (temperature of the climatic chamber). The maximum temperature reached by the FPGA at 95 °C of the climatic chamber was around 120 °C, with slight variations from board to board. The minimum temperature reached by the FPGA was around -12 °C, temperature measured when the temperature of the chamber was -40 °C. During all the temperature steps the boards behaved correctly and not errors were identified.

The power consumption increased as expected with temperatures higher than 50 °C, but even with these levels of power consumption, the boards behaved correctly.

Also, the six boards behaved correctly after modifying the extreme temperature stress tests.

The CLBv4 and PBv4 boards passed successfully the HALT tests and no errors were detected, validating the design.

4. Conclusions

A new version of the Central Logic Board and Power Board has been designed, in order to add new functionality, improve the oscillator system, and increase reliability and efficiency. The FIDES analysis has been performed on these two new designs. Six pairs of boards have undergone the HALT tests, performing well in the range of temperatures applied (-40 °C to 100 °C). The FIDES analysis and the tests performed show that the acquisition boards support a high level of stress, which provides guarantees for their use during the life of the KM3NeT experiment. A complete functional test bench replicating one of the DU of KM3NeT is being installed at the moment, and is foreseen to perform a Preproduction Readiness Review of the boards this year, starting mass production of the CLBv4 and PBv4 soon after.

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