PROCEEDINGS OF SCIENCE

Development of the Configuration, Calibration and Monitoring System of the New Small Wheel Electronics for the ATLAS experiment

Polyneikis Tzanis[a,b,*] **on behalf of the ATLAS Muon Collaboration**

[a] *National Technical University of Athens, Heroon Polytechniou 9, Zografou, Greece*

[b] *Brookhaven National Laboratory, Upton, NY 11973-5000, U.S.A.*

E-mail: polyneikis.tzanis@cern.ch

A series of upgrades are planned for the LHC accelerator to increase the instantaneous luminosity to $7.5 \times 10^{34} cm^{-2} s^{-1}$. The luminosity increase drastically impacts the ATLAS trigger and readout data rates. The present ATLAS Small Wheel Muon detector will be replaced with a New Small Wheel (NSW) detector which is expected to be installed in the ATLAS underground cavern by the end of the Long Shutdown 2 of the LHC. One crucial part of the integration procedure concerns the installation, testing and validation of the on-detector electronics and readout chain for a very large system with a more than 2.1 M electronic channels in total. These include 7K Front-End Boards (MMFE8, SFEB, PFEB), custom printed circuit boards each one housing eight 64-channel VMM Application Specific Integrated Circuits (ASICs) that interface with the ATLAS Trigger and Data Acquisition (TDAQ) system through 1K data-driver cards. The readout chain is based on optical link technology (GigaBit Transceiver links), which is a newly developed system that will serve as the next generation readout driver for ATLAS that connects the backend to the front-end electronics via the Front-End LInk eXchange (FELIX). For the configuration, calibration and monitoring path, the various electronics boards are supplied with the GBT-SCA ASIC (Giga-Bit Transceiver-Slow Control Adapter) which is part of the Gigabit Transceiver Link(GBT) chipset and its purpose is to distribute control and monitoring signals to the electronics embedded in the detectors and in the ATLAS service areas. Experience and performance results from the first large-scale electronics integration tests performed at CERN on final NSW sectors will be presented.

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1. The New Small Wheel

The LHC accelerator will be upgraded to deliver an instantaneous luminosity up to $7.5 \times 10^{34} cm^{-2} s^{-1}$. The luminosity increase dramatically impacts the ATLAS[1] trigger and readout data rates. The present ATLAS small wheel muon detector will be replaced with a New Small Wheel (NSW)[2] which is expected to be installed in the ATLAS at the end of 2021. A graphic representation is displayed on Fig. 1. With the series-production of 16 Micromegas (MM)[3] and small-strip Thin Gap Chambers (sTGC) modules completed, the integration of the modules into the final, fully-equipped New Small Wheel sectors are currently underway at CERN.

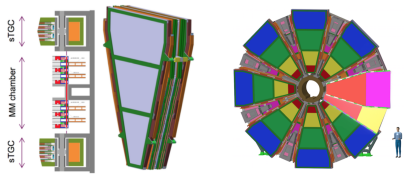

Figure 1: A graphic representation of the NSW sector (left) that consists of 8 layers of Micromegas in the inner part sandwiched between 4+4 layers of sTGC detectors in the outer parts, and a view of the NSW[2] (right) with 16 sectors in total.

2. Electronics Overview

The NSW electronics for the trigger and Data Acquisition (DAQ) path of both detectors can be divided into two major categories, on-detector and off-detector electronics as shown on Fig. 2. The on-detector electronics Front-End boards, Level-1 Data Driver and ART Data Driver Card will be placed inside the cavern (detector area with radiation and magnetic fields) and consist of custom-made boards using radiation-tolerant Application Specific Integrated Circuits (ASICs). The communication between these boards will be established with the use of mini Serial Attached

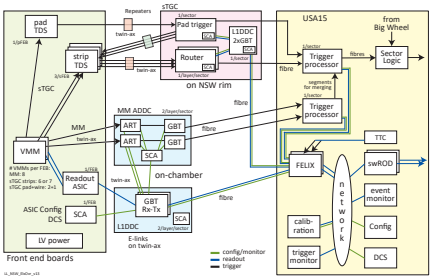

Figure 2: Overview of the on/off-detector electronics and the DCS, Configuration and Calibration path via the SCA, the FELIX and the SCA OPC UA Server. A common readout path and a separate trigger path are developed for each detector technology. [8]

Small Computer System Interface cables. The off-detector electronics (Front End LInk eXchange (FELIX), trigger processor, sector logic and services running on commercial server computers like Read Out Drivers (ROD), Detector Control System (DCS)[4], event monitoring, configuration, trigger monitor and calibration) will be placed outside the cavern in an area that is called USA15.

3. FELIX & GBT-SCA & SCA OPC UA Server

The keystone of the ATLAS DAQ system will be the FELIX which is an FPGA-based system housed by a commercial server. FELIX will essentially be a bridge between the front-end electronics of all ATLAS detector subsystems, and their corresponding back-end components, which will mostly be software-based. Situated in the USA15, FELIX connects to the front-end electronics of the ATLAS cavern via optical links, or GBT[5] links, each one of which is running at 4.8 Gb/s. For the NSW case, FELIX will interface with the front-end nodes over 24 optical links. These links carry the GBT frame, which is 84-bit wide. The Giga-Bit Transceiver (GBT) protocol is a transmission scheme that involves radiation-tolerant ASICs that are capable of handling the large amounts of data of high energy physics experiments. The GBT-SCA ASIC (Giga-Bit Transceiver-Slow Control Adapter)[6] is part of the GBT chipset and is usually connected both to a GBTx and to several front-end devices. Its purpose is to distribute control signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters as shown on Fig. 3. In order to meet the requirements of different front-end ASICs used in high-energy physics experiments, it provides various user-configurable interfaces, such as SPI, I2C or JTAG, and is capable of performing simultaneous operations. In this SCA-GBTx-FELIX communication chain[8], the last two components can be viewed as data mediators, so there is one piece missing: the back end logic that actually builds the packets-to-be-transmitted to the SCA, and handles the inbound traffic from the ASIC. This is a software suite, which is a dedicated Open Communications Platform Unified Automation (OPC UA) server.

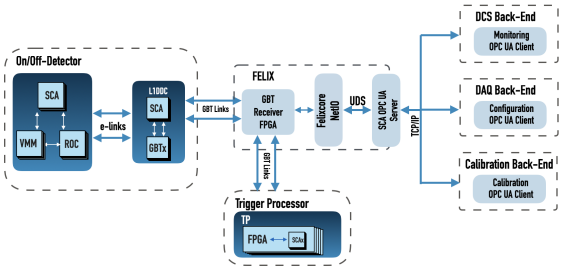

Figure 3: Overview of the calibration/configuration/monitor path.

4. Configuration

The NSW is a fully autonomous trigger and tracking detector system, adequately supported by an advanced electronics scheme and ready to handle the challenges of increased instantaneous luminosity at the High Luminosity LHC. It includes more than 60k front-end ASICs and a few tens of FPGAs, which need to be configured before every run of the experiment. This process needs to be efficient and quick, since it needs to happen a few times per day. The main ASIC to be configured is the VMM[7], the front-end signal pre-processing chip that can readout 64 channels. A few kbytes of configuration data include thresholds for each channel, but also global registers to define the gain, time-to-amplitude conversion and many others. For this procedure we need to use the SCA's SPI master to communicate with the 8 SCA's SPI slaves in the VMMs. Also, the SCA's

GPIO interface is required, to act as an enable signal. Moreover, a similar scheme using the SCA's I2C interface is used for configuration of the TDS chip, which is used for timing and trigger.

5. Calibration

The calibration procedure consists of various timing and charge calibrations of the front-end electronics. Gain calibration is done by varying the signal input using the internal pulser of the chip as shown on Fig. 4. A specific configuration file needs to be loaded on the VMM chips, which is done with the SCA. Calibration of a time-to-amplitude converter is done by skewing the input clock, which is performed by re-configuring the specific on-board with different settings. Baseline and noise level is defined by reading out each channel output with the ADC when no collisions are occurring.

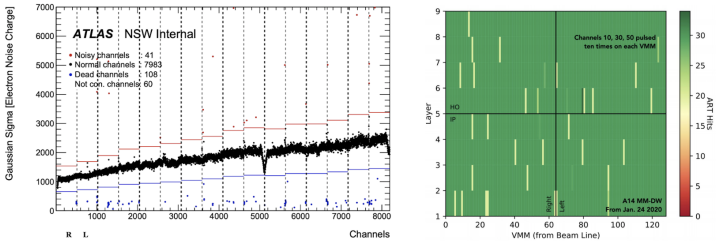

Figure 4: Left: Noise baseline measurement, Right: Automated ART test plot produced during trigger path validation. All VMM channels are pulsed sequentially and produce a map of the ARTs that are read out in the TP.[2]

6. Monitoring

Due to its complexity and long-term operation, the ATLAS detector requires the development of an advanced DCS for the electronics monitoring using the SCA chip, which is installed on the 8000 front-end boards of the NSW. The use of such a system is necessary for the safe operation of the detector as well as to act as a homogeneous interface to all the sub-detectors and the technical infrastructure of the experiment. This system gives us the ability to monitor all the power/temperature sensors, on-chip temperature and information, which are connected to the SCA on all the front-tend boards of the NSW, as shown on Fig. 5.

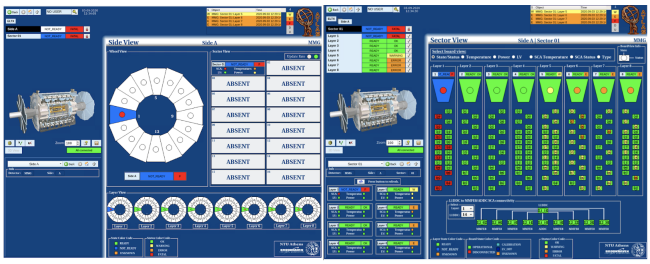

Figure 5: The DCS FSM and panels for the NSW Electronics monitoring.

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