

ATLAS Level-0 Endcap Muon Trigger for HL-LHC

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The design of the Level-0 endcap muon trigger for the ATLAS experiment at High Luminosity LHC and the status of the development are presented. High Luminosity LHC is planned to start the operation in 2027 with an instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. In order to cope with the proton-proton collision rate higher than that of LHC, the trigger and readout systems need to be replaced. The new Level-0 endcap muon trigger system is required to reconstruct muon candidates with an improved momentum resolution to suppress the trigger rate with keeping efficiency. That can be achieved by combining signals from various subdetectors, thin gap chambers, resistive plate chambers, micromesh gaseous detectors, and scintillator-steel hadronic calorimeters, to form more offline-like tracks. The performance of the Level-0 endcap muon trigger was evaluated with software and the firmware development is ongoing.

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1. Introduction

The ATLAS detector [1] is a general-purpose detector at the Large Hadron Collider (LHC), investigating a wide range of physics. High Luminosity LHC (HL-LHC) is an upgrade of LHC to achieve higher luminosities, thereby enabling experiments to reach better physics sensitivity. Operation of HL-LHC is scheduled to start in 2027 with an instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. As the instantaneous luminosity is increased to its ultimate configuration, the experiment needs to cope with about 200 proton-proton collisions per bunch crossing. In order to handle this high luminosity, the trigger and readout systems are planned to be upgraded [2]. This paper describes design and development status of the Level-0 endcap muon trigger of the ATLAS experiment at HL-LHC.

2. Level-0 endcap muon trigger scheme for HL-LHC

In the original trigger scheme for the first level of the muon trigger, muon track candidates are identified by a simple coincidence logic in on-detector boards using hits from the Thin Gap Chamber on the Big Wheel (TGC BW). TGC is a multi-wire proportional chamber which measures two-dimensional position using signals from wires and strips orthogonal to the wires. TGC BW consists of three stations. Stations M1, M2 and M3 have three, two and two layers, respectively, as shown in Figure 1a. The transverse momentum (p_T) of muon candidates is evaluated by look-up tables implemented on Sector Logic boards (SL). The main source of background in the endcap muon trigger system is low-momentum charged particles emerging from large amounts of dense material such as the toroid coils, beam pipe and shield (“fake muons”). Triggers by the fake muons are suppressed by combining signals from various inner subdetectors: TGC in the endcap inner station (TGC EI), Resistive Plate Chambers in the barrel inner station (RPC BIS78), New Small Wheel (NSW), and Tile hadronic calorimeter (TileCal) as shown in Figure 1a and Figure 1b.

In the new Level-0 endcap muon trigger for HL-LHC, muon track “segment” reconstruction using full-granular information will be enabled by transferring all hit information from the TGC BW to SL. In addition, complex coincidence algorithms will be implemented to improve p_T resolution. After the muon track candidates are provided by TGC BW and the inner subdetectors, the Monitored Drift Tube (MDT) is used to improve the p_T resolution at the Level-0 muon trigger. Main functions of SL are implemented on the Virtex UltraScale+ FPGA provided by Xilinx.

3. TGC track segment reconstruction

Muon track segments are reconstructed in TGC with a “pattern matching” algorithm that compares with predefined TGC hit lists for high- p_T muons. Each predefined hit pattern has angle and position associated to a track segment. In the trigger scheme in Run-3, at least two (one) hits in the inner three (two) layers and at least three hits in the outer four layers for wires (strips) are required for the high- p_T muons. In the endcap SL for HL-LHC, a looser coincidence with at least five (four) hits in the seven (six) layers for wires (strips) is required to improve the efficiency. The new trigger scheme is expected to improve the trigger efficiency by 4.2% compared to the current trigger scheme. Track segments are reconstructed with an average angular resolution of 4 mrad.

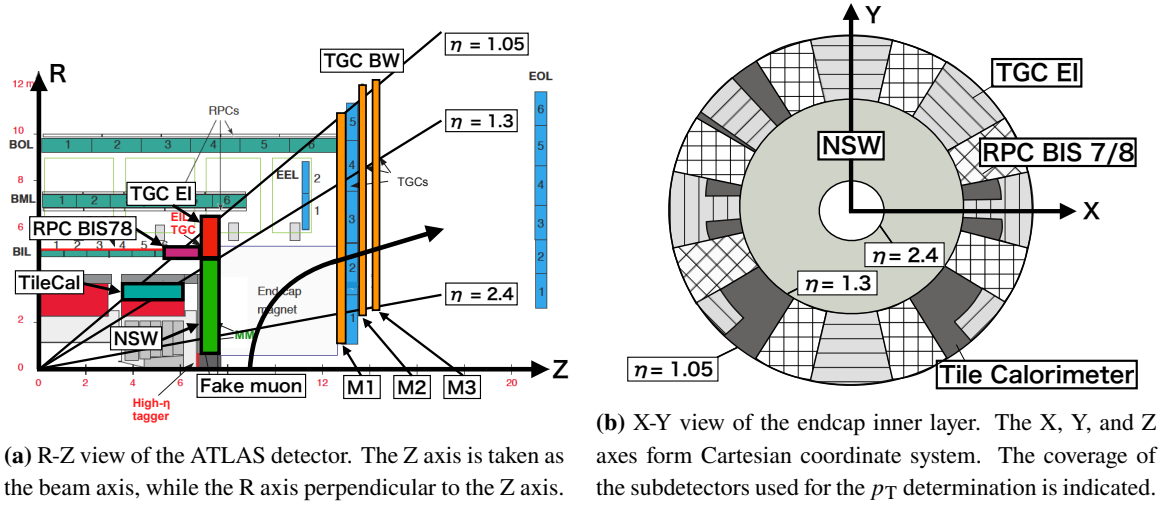


Figure 1: Layout of the ATLAS muon spectrometer. [3]

4. Trigger scheme using inner detectors

Muon candidates in the trigger system are provided by combining the TGC track segments reconstructed in TGC BW and the information from the inner subdetectors. In the region with $1.05 < |\eta| < 1.3$, p_T is determined by the position difference between TGC BW track segments and hits in the TGC EI, RPC BIS78 and TileCal. In the region with $1.3 < |\eta| < 2.4$, p_T is determined by the position difference between the TGC BW track segments and the tracks reconstructed in NSW.

5. Improvement of trigger performance

Trigger performance of the Level-0 endcap muon trigger (not including the more precise p_T measurement in MDT) was evaluated. As shown in Figure 2a, higher efficiency ($\sim 4\%$) in the plateau region and better rejection for the low p_T muons compared to the Run-2 trigger are obtained, thanks to the looser coincidence and the good angular resolution, respectively. Figure 2b shows that the obtained trigger rate for 20 GeV threshold is about 23 kHz at the luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, which is the nominal value of HL-LHC. Further rate reduction by $\sim 50\%$ in the next step with MDT is expected [2].

6. Firmware design

The firmware consists of four modules as listed below.

- 1) *Wire (Strip) Segment Reconstruction* : To reconstruct track segments with a pattern matching algorithm using all wire (strip) hits from the TGC BW.
- 2) *Wire-Strip Coincidence* : To combine wire and strip track segments from the Wire and Strip Segment Reconstruction modules to evaluate p_T of muon candidates.
- 3) *Inner Coincidence* : To combine track segments from the Wire-Strip Coincidence module with information from inner detectors to evaluate p_T with higher precision.

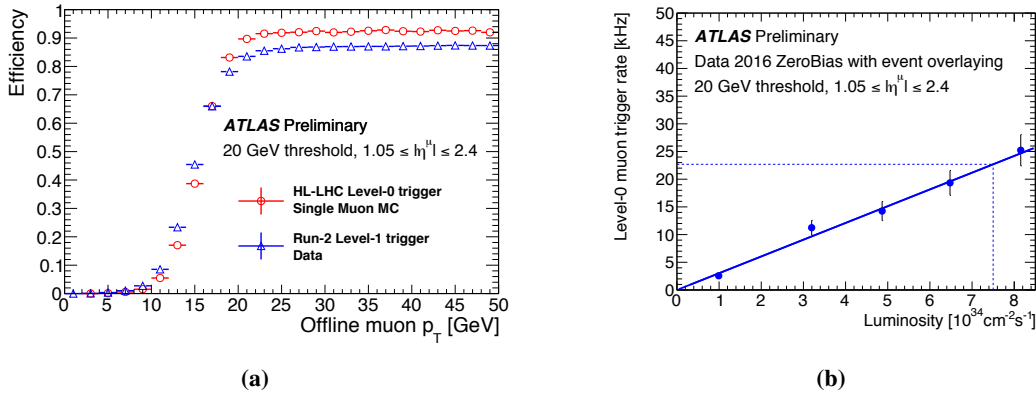


Figure 2: (a) Expected efficiency for the Level-0 muon trigger with the HL-LHC scheme (red) and with the Run-2 scheme (blue). (b) Estimated rate of the Level-0 single muon trigger at HL-LHC based on TGC, TileCal, and NSW for a pseudorapidity range $1.05 < |\eta| < 2.4$ and a p_T threshold of 20 GeV. [4]

4) Track Selector : To send three muon candidates with the highest- p_T to the MDT. After the precise measurement in MDT, the Track Selector module receives muon candidates with updated p_T and transfers them to the Muon to Central Trigger Processor Interface (MUCTPI).

7. Performance evaluation of the firmware

The performance of the Level-0 muon trigger for HL-LHC is evaluated and it showed higher efficiency and better rejection for the low p_T muons, compared to the current system. A test firmware of TGC pattern matching algorithm for a specific unit has been implemented in an FPGA with an evaluation board VCU118. The performance has been evaluated by injecting test vectors of TGC hits obtained from Monte-Carlo (MC) sample and used as the FPGA inputs. The angular resolution estimated from the offline analysis is reproduced in the test. Development of full chain firmware for limited coverage is in progress.

References

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