

## The Particle Flow Algorithm in the Phase II Upgrade of the CMS Level-1 Trigger

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The CMS experiment has greatly benefited from the utilization of the particle-flow (PF) algorithm for the offline reconstruction of the data. The Phase II upgrade of the CMS detector for the High Luminosity upgrade of the LHC (HL-LHC) includes the introduction of tracking in the Level-1 trigger, thus offering the possibility of developing a simplified PF algorithm in the Level-1 trigger. We present the logic of the algorithm, along with its inputs and its firmware implementation. We show that this implementation is capable of operating under the limited timing and processing resources available in the Level-1 trigger environment. The expected performance and physics implications of such an algorithm are shown using Monte Carlo samples with high pile-up, simulating the harsh conditions of the HL-LHC. New calorimeter features allow for better performance under high pileup (PU) to be achieved, provided that careful tuning and selection of the prompt clusters has been made. Additionally, advanced pile-up techniques are needed to preserve the physics performance in the high-intensity environment. We present a method that combines all information yielding PF candidates and performs Pile-Up Per Particle Identification (PUPPI) capable of running in the low latency level-1 trigger environment. Demonstration of the algorithm on dedicated hardware relying on ATCA platform is presented.

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## 1. Introduction

The main goal of the High Luminosity LHC (HL-LHC) upgrade is to enhance the performance of the current LHC to increase the prospects of new physics discoveries. To tackle the challenges erected by an increase in the luminosity and high pileup, CMS and its sub-detectors, including Level-1 Trigger, will undergo a massive upgrade. Several changes were devised for this upgrade viz., the replacement of the end-cap calorimeter by high-granularity calorimeter (HGCAL) and, the inclusion of the tracker data to the Level-1 Trigger architecture. With these increased arsenals of information and latency at the L1 trigger, the implementation of the particle-flow (PF) algorithm is now a reality at the hardware fabric of CMS Level-1 trigger system. A pileup mitigating algorithm called Pileup Per Particle Identification (PUPPI) will also be deployed at the Level-1 Trigger.

## 2. Calorimeter Trigger System

The calorimeter trigger system is one of the main backbone of the PF approach, along with the tracker. This system receives its input in the form of trigger primitives from the back-end electronics of four calorimeter sub-detectors. The barrel calorimeter trigger primitives are processed in two steps viz., regional calorimeter trigger (RCT) and global calorimeter trigger (GCT). RCT takes inputs from barrel electromagnetic calorimeter (ECAL) and barrel hadronic calorimeter (HCAL) and sends the information to the next level Global Calorimeter Trigger (GCT) for further processing. GCT, takes information from barrel calorimeter (ECAL and HCAL) through RCT and also receives inputs from endcap calorimeters (HGCAL) and HF. The information from all the detectors is combined in GCT and then physics objects  $E_{\text{Gamma}}$ , jets and taus are created. GCT compiles the hadronic forward (HF) and RCT information and sends it to the Correlator Trigger (CT), which hosts the particle-flow algorithm. As a demonstration, the RCT and GCT firmwares are deployed in Phase-1 based Xilinx Virtex-7 calorimeter trigger processor (CTP7) cards, which supports 48 input-output links, running at 10 Gbps. The RCT and GCT algorithms, clocked at 160 MHz are synthesized in Vivado-HLS, resulting a total latency of 10 and 18 LHC bunch-crossing respectively. The firmware of the RCT algorithm is also implemented in the Phase-2 hardware demonstrator called APd1 card based on the ATCA form factor. The latency of 66 (40) clock cycles is achieved for 360 (240) MHz clock. The detailed logic utilization of the RCT and GCT firmwares are presented in Table 1.

Algorithm	LUT (%)	FF (%)	BRAM (%)	DSP (%)
RCT (CTP7)	22	17	0	0
RCT (APd1)	4	3	0	0
GCT	48	30	0	0

**Table 1:** Resource Utilization for RCT and GCT in Virtex 7 and VU9P FPGA

## 3. Particle-flow: Design and Firmware Implementation

The availability of the tracker and the high-granular data from calorimeter throughout the Phase-II upgrade enables the implementation of the particle-flow and the PUPPI algorithm at the Level-1 Trigger. The proposed architecture of the L1 trigger is shown in figure 1.

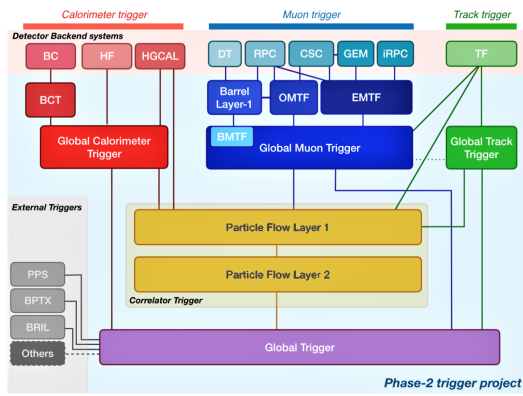


Figure 1: CMS Phase-2 L1 trigger design.

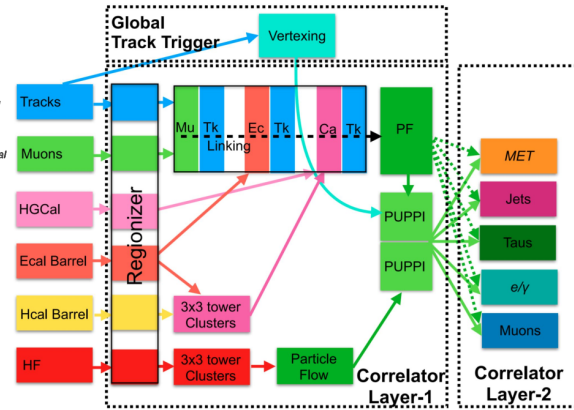


Figure 2: Correlator trigger organization.

The particle flow algorithm along with PUPPI is implemented at the Correlator Trigger (CT) cards. CT is implemented in two layers with first layer, termed as "Layer-1" mainly constitute the PF and PUPPI algorithm and produces the PF candidates by utilizing the calorimeter and tracker information, and a second layer, referred to as "Layer-2", performs sorting and building final trigger objects for the Global Trigger (GT). In the PF algorithm, the best-resembled track in the tracker by  $\Delta R$  and  $p_T$  is flagged as muon for each standalone input muon object. The unsettled tracks information is then tagged with the calorimeter. PUPPI is also implemented at the Correlator Layer-1, depends on the use of vertexing to mitigate the contribution of the pileup at the scale of particles. Fig 2 represents the CT architecture. For an efficient FPGA implementation, the Regionizer algorithm is used to supervise all the input and tagged it with its corresponding regions before applying it to the PF algorithm. The Regionizer firmware is implemented and compared with its equivalent software implementation as shown in figure 3. In the quest of designing the PF+PUPPI system efficient in processing the complete detector geometry at the LHC bunch-crossing frequency of 40 MHz, various possible region sizes, pipeline intervals, and the logic resources required for these firmware implementations are determined and shown in fig 4.

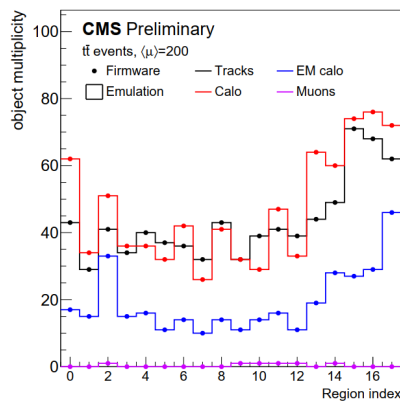


Figure 3: Regionizer firmware and software emulation.

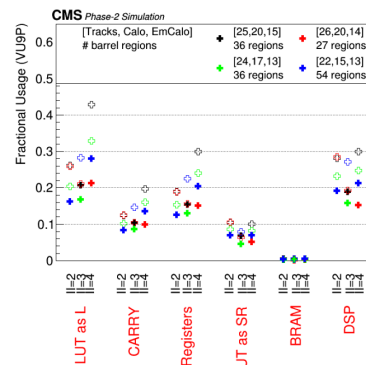
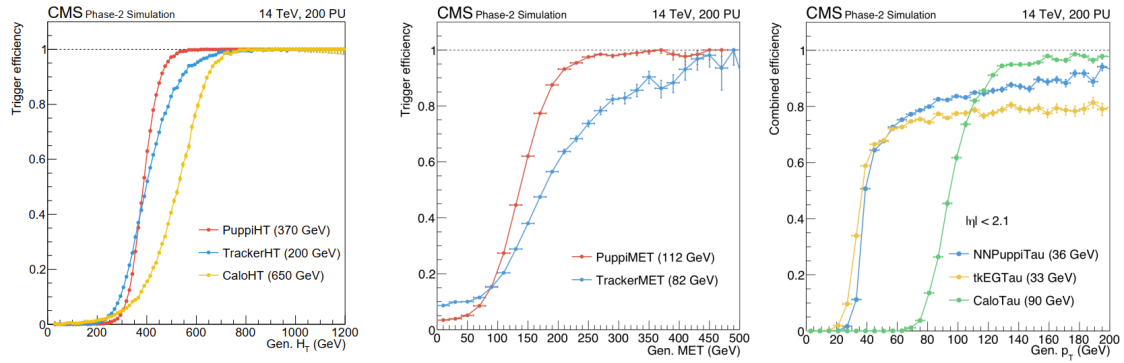


Figure 4: Fractional utilization of VU9P FPGA resources required to process the input from barrel with PF and PUPPI firmware at 40 MHz.

#### 4. Particle-flow: Performance

The PF and PUPPI algorithm is used in pursuit to improve the performance of the L1 trigger in comparison with the standalone calorimeter or track-only objects. For missing transverse energy (MET) triggers, PUPPI implementation achieved an efficiency of 95% at a threshold approximately 200 GeV lower than track-only trigger. In the case of  $H_T$  (scalar gross of the  $p_T$  of all jets), application of PUPPI demonstrate a sharper turn-on. PUPPI also improved the performance of hadronic tau lepton trigger by reducing the turn-on by approximately 40 GeV. Figure 5 shows the summary of these achieved results.



**Figure 5:** Plots of the improved performance feasible by employing PF+PUPPI objects in contrast to calorimeter- or track- only objects for  $H_T$  (left), MET (center), and hadronic tau lepton (right) triggers.

#### References

- [1] The Phase-2 Upgrade of the CMS Level-1 Trigger. Technical Report CERN-LHCC-2020-004. CMS-TDR-021, CERN, Geneva, Apr 2020. URL <http://cds.cern.ch/record/2714892>.

#### Acknowledgement

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