ATLAS LAr Calorimeter Commissioning for LHC Run-3

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Liquid argon (LAr) sampling calorimeters are employed by ATLAS for all electromagnetic calorimetry in the pseudo-rapidity region $|\eta| < 3.2$, and for hadronic and forward calorimetry in the region from $|\eta| = 1.5$ to $|\eta| < 4.9$. After detector consolidation during a long shutdown, Run-2 started in 2015 and about $150\,\text{fb}^{-1}$ of data at a center-of-mass energy of $13\,\text{TeV}$ were recorded. Installation of the Phase-I detector upgrades began after the end of Run-2. New trigger readout electronics of the ATLAS Liquid-Argon Calorimeter have been developed. Installation began at the start of the LHC shut down in 2019 and is expected to be completed in 2021. A commissioning campaign is underway in order to realise the capabilities of the new, higher granularity and higher precision level-1 trigger hardware in Run-3 data taking. This contribution will give an overview of the new trigger readout commissioning, as well as the preparations for Run-3 detector operation

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1. The ATLAS Liquid Argon Calorimeter

The ATLAS Liquid Argon (LAr) calorimeter [1, 2] is a sampling calorimeter with full azimuthal coverage. The calorimeter is divided in different sub-detectors as sketched in Figure 1a: a high granularity Electromagnetic Barrel (EMB) with accordion geometry covers the pseudo-rapidity region $|\eta| < 1.475$, two Electromagnetic EndCap (EMEC) cover the region $1.375 < |\eta| < 3.2$ while two Hadronic EndCap cover the region $1.5 < |\eta| < 3.2$; finally, two Forward Calorimeters (FCal) can detect particles up to $|\eta| = 4.9$. Each sub-detector is longitudinally segmented in three layers, referred as front, middle and back; for regions with $|\eta| < 1.8$ an additional thin layer called "presampler" is emplaced which is used to recover upstream energy loss. Three different cryostats enclose the barrel and two EndCap parts respectively: those maintain the Liquid Argon at 88 K to use it as the active medium of the detector, while various absorbers with high Z are used as passive medium.

1.1 Main readout and legacy L1 trigger

To collect the ionization signal produced in the LAr gap shown in Figure 1b, a high electric field is applied across the gap and a triangular-shaped pulse is produced. The signal is readout from more than 180 000 channels and routed outside the cryostats towards the Front End Crates (FEC). The Front End Boards (FEB) [3] are responsible for receiving up to 128 analogue channel signals from one layer. The signal is first amplified with three different gains and then shaped with a bipolar CR-(RC)^2 analogue filter, producing the form shown in Figure 1c. The shaped signal is then sampled at the LHC bunch-crossing frequency of 40 MHz and stored in a Switched Capacitor Array (SCA) analogue memory buffer, while awaiting for the Level-1 (L1) trigger accept. When this arrives, the signal is digitized and transmitted to the back end, consisting of Readout Drivers (ROD) housed in the service cavern and connected via optical links.

In addition, the FEB sums analogically the signals via the mezzanine Layer Summing Boards (LSB). These sums are then routed by the FEC baseplane to the Tower Builder Boards (TBB), which sum data from all layers in the so-called Trigger Towers (TTs), corresponding to detector slices of $\Delta\eta \times \Delta\phi \sim 0.1 \times 0.1$. The full detector is therefore covered with ~5400 TTs and the information
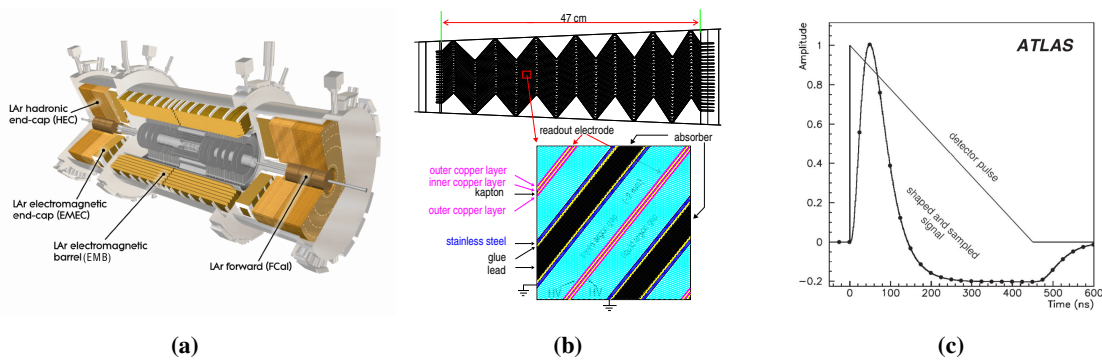

Figure 1: (a) Schematic view of the different sub-detectors composing the ATLAS Liquid Argon system. (b) Accordion geometry for the electromagnetic calorimeter and LAr gap served with HV lines. (c) Triangular pulse produced in the LAr gap compared to the shaped and sampled signal sent of the main readout. [2]
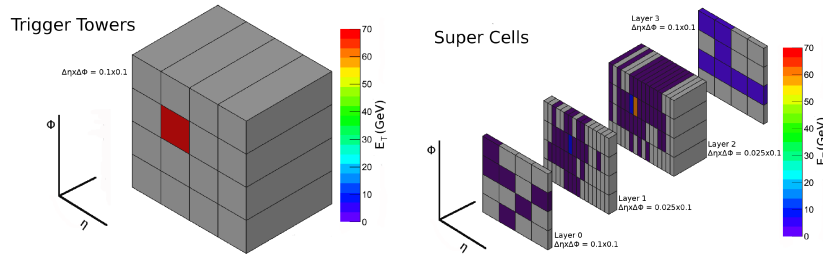
Figure 2: Simulation of the energy deposits of a 70 GeV electron reconstructed with the Run-2 Trigger Towers (left) and compared to the new Super Cells based L1 trigger to be used during Run-3 (right). [5]

on the longitudinal shower development is lost. The TTBs send the analogue TT signals to the L1 trigger systems [4] in the back end, which computes the L1 accepts to be sent back to the LAr system.

2. Digital trigger readout upgrade

With the planned restart of LHC operations in 2022, the overall detector occupancy will increase compared to the Run-2 conditions. On the other hand, the collaboration has decided to keep the L1 and High Level Trigger (HLT) rates to the same Run-2 levels of 100 kHz and 1 kHz respectively. Therefore, in order to maintain the same Run-2 physics performance, an upgrade of the L1 trigger system is required [5]. New Feature Extractor (FEX) modules [6] have been designed to use topological shower shape information coming from the detector and upgraded L1 algorithms, in order to better discriminate among different physics objects. After the Phase-I upgrade, calorimetric cells will be grouped into ~34 000 "Super Cells" (SC), which provide higher cells granularity and the longitudinal information coming from the LAr four layers. Figure 2 shows a depiction of an electron energy deposit as seen through a TT compared to the same deposit measured by a SC for a typical EM (η, ϕ) slice. In this case, the SCs provide the same $\Delta\eta \times \Delta\phi$ information for the presampler and back layers but a $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ information for the front and middle layers; moreover no sum is performed over the layers. Given the higher granularity provided by SCs, L1 algorithm will be able to use shower shapes development variables to discriminate among different physics objects. The discrimination provided by them is sketched in Figure 3a: using this information will allow to keep the same trigger rate and thresholds as during Run-2 even in the harsher Run-3 environment as shown in Figure 3b. Moreover, improved L1 EM resolution will substantially sharpen the trigger turn-on curves and therefore will lead to a reduced offline E_{T} threshold and to an increase of acceptance.

2.1 Readout electronics

To be able to provide higher granularity information with respect to the legacy L1 trigger used during Run-2, both front end and back end electronics have been upgraded. Figure 4 shows a schematic overview of the readout electronics, with the new changes highlighted in orange.
The most notable difference is the inclusion of the LAr Trigger Digitiser Boards (LTDB), which are in charge of processing and digitizing the SC analogue signals. In order to accommodate these new boards, the baseplanes in each FEC must be replaced with one with additional slots. The
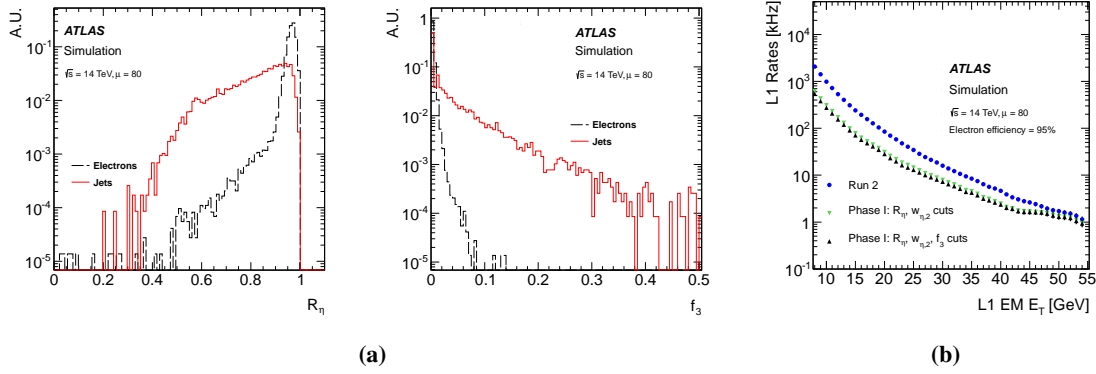
Figure 3: (a) Electromagnetic or hadronic showers can be discriminated with the help of the shower shape variables $R_\eta = \frac{E_{3\times2}}{E_{7\times2}}$ and $f_3 = \frac{E_{S3}}{E_{tot}}$. (b) Expected L1 trigger rates for an instantaneous luminosity of $3 \times 10^3 \, \mathrm{cm^{-2}\,s^{-2}}$ as a function of the EM E_T threshold for the case of the Run-2 electronics (blue) and the upgraded digital trigger with different selections of shower shape variables (black and green). The trigger rate for the selection of electrons at 95% efficiency was 20 kHz during Run-2 for a E_T threshold of 20 GeV that can only be reached by using additional shower information. [5]
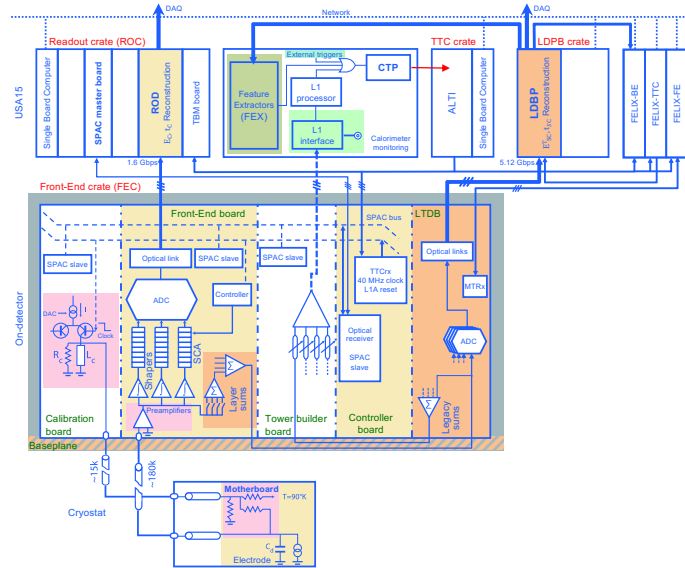

Figure 4: The ATLAS LAr calorimeter electronic architecture as of LHC Run-3. The new boards are the Baseplane, the Layer Sums boards, the LTDB and LDPB, which are highlighted in orange ▮. This diagram depicts the EM calorimeters; slight changes would be needed to describe the HEC and FCal electronics.

new baseplanes are also needed to operate the legacy and digital triggers concurrently, to ease the new system commissioning and have a fallback solution in case of unforeseen issues. Each LTDB receives the analogue signals via the baseplane from the LSB, which has been upgraded to provide more granular analogue sums required for SCs. Each LTDB can process up to 320 SC signals thanks to custom-designed 12 bit ADC working at 40 MHz, constructed in 130 nm TSMC technology and with the least significant bit being 150 MeV and 300 MeV in front and middle layers respectively. The custom design is dictated by the radiation hardness required to run the LTDBs for

HL-LHC too. The LTDB further sums up the analogue signal in order to feed the legacy TTB with the desired granularity. In addition, the LTDB transmits the SC signals to the back end via optical links: each fiber transmits 8 SCs at 5.12 Gb/s thanks to the custom-designed LOCld laser drive, after serialisation performed by the LOCx2 device, both built with a 250 nm Silicon-On-Insulator technology.

The reception of this digital SC data and its transmission to the new FEXes is handled by new back end hardware, collectively called LAr Digital Processing System (LDPS). This system receives ADC data and align timing, computes E_T for individual SCs, identifies the bunch cross and sends the result to the L1 trigger modules. The LDPS consists LAr Digital Processing Blades (LDPB), each built-in Advanced Telecommunications Computing Architecture (ATCA) format and comprises one ATCA carrier named LAr Carrier (LArC) and up to four LAr Trigger prOcessing MEzzanines (LATOMEs). The hardware control and monitoring of each blade proceeds via an Intelligent Platform Management Controller (IPMC) plugged into the LArC. The LATOMEs get the ADCs via optical links (25 Tbps in total) for each brunch crossing (40 MHz) and compute the corresponding energies, then they transmit the elaborated data to L1Calo trigger (41 Tbps in total). Given the strict latency time, the LATOME and LArC are operated by high-performance commercial FPGAs Intel Arria-10 and Xilinx Virtex 7 respectively.

2.2 Installation status

During the Long Shutdown (LS2) of the LHC, the installation of the new front end and back end LAr electronics has progressed. All the boards in the FEC have been removed and brought to the surface, where new LSBs have been installed on the FEBs. Simultaneously, the cooling plates surrounding each board were replaced with newly manufactured ones, as well as the aging hoses that supply cold water to each board. Then FEBs, TTBs and the new LTDBs have been reinstalled in the FEC on the new baseplane. The LDPS back-end installation proceeded in parallel in the ATLAS service cavern. LDPBs have been installed concurrently to the equivalent LTDBs, with data fibres fully connected between the LTDBs and LATOMEs for all of the ATCA crates. Monitoring and control system have been put in place and included in the ATLAS main control system.

At the time of this publication, the installation is completed. In total, on the front end side, 124 LTDBs of seven different flavours have been installed on 114 new baseplanes. All the FEBs have been refurbished with 2968 LSBs of six different flavours depending on the detector region. Concerning instead the back end, 30 LDPBs, corresponding to 30 LArCs and 116 LATOMEs have been installed in the three ATCA shelves.

2.3 Commissioning status

Although the main readout path is unchanged by the Phase-I upgrade, additional routing and refurbished electronics are now employed. Moreover, FEBs have been returned to different positions within the various FECs. Therefore, it is important to confirm that the main readout is performing as before the installation. Connectivity scans are run to ensure that the FEBs are connected to the channels properly, full calibration sets are taken and compared to the reference runs from the end of Run-2. These provide detail information on noise levels and calibration coefficients and the system demonstrated to perform as well as before: no change in electronic noise level after FEBs refurbishment have been found and the calibration results are unchanged. As an example, the noise
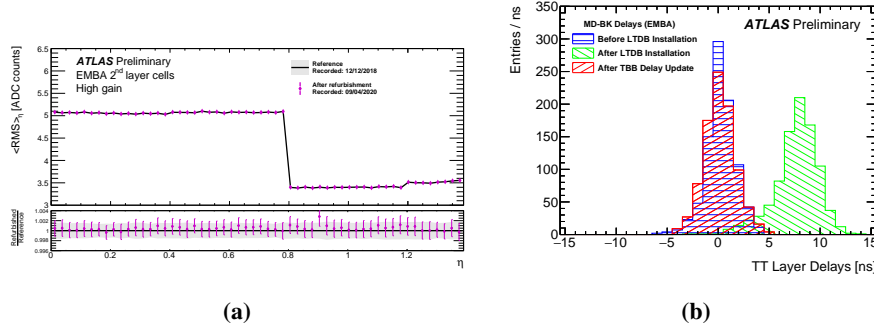
(a)   (b)

Figure 5: (a) Mean value of the RMS in ADC counts for the cells in a given pseudorapidity (η) range. The black line shows the values measured at the end of Run 2 while the purple dots the values measured after the installation during LS2. The displayed uncertainties are computed as $\sigma_{rms,cells}/\sqrt{N_{cells}}$, where $\sigma_{rms,cells}$ and N_{cells} are the RMS of the RMS values over the cells and the number of cells in the given η range respectively. The step at $\eta = 0.8$ is due to the change of the electrodes geometrical structure. (b) The delays of signals from the back layer (BK) with respect to the middle layer (MD) introduced by the LTDB installation for the L1 TT signals at the arrival in the L1Calo system. [7, 8]

level as a function of η in the middle layer of the EMB is reported in Figure 5a.

Concerning legacy trigger readout path, the analogue sums will be routed through the LTDBs before reaching the TTBs. This increased path will introduce a delay in the L1 system for reception of the signal between different layers, which must be measured and accounted for in the trigger decision. Moreover, the introduced timing shifts should reflect the expected changes in the system. After refurbishment of each crate, gain and timing scans are taken to check the connectivity and to measure the delay between the sums from different layers, with an example provided by Figure 5b. A timing difference of up to 10 ns is observed between some layers, which is consistent with the expected change due to the increased path through the LTDB.

In order instead to validate the digital trigger readout path both on the front end and back end, different calibrations runs are taken and compared to the LAr main readout path: in particular, delay runs consist of injecting pulses with a single input signal current (DAC) with an increasing time shift in steps of 1.04 ns in order to reconstruct the full pulse shape as shown in Figure 6a; on the other hand, ramp runs, where signals of increasing DAC are injected, provide the gain slope, which is extracted from a fit of the DAC versus ADC curve. Figure 6b shows that the ADC increases linearly with deposited transverse energy up to ~800 GeV, where an expected saturation of the SC pulse occurs. From these runs, calibration constants used for energy reconstruction are obtained, and the offline E_{T} can be compared to what is computed by the LATOME: the comparison leads the observed differences below 1% representing a good overall agreement.

3. Conclusion

In this contribution, the ATLAS LAr digital trigger system has been described and an overview of the installation and commissioning status has been given. Despite the challenges brought on by recent global events, the installation is completed and the commissioning is still ongoing, but excellent results have been obtained so far. The main readout and the legacy trigger path will
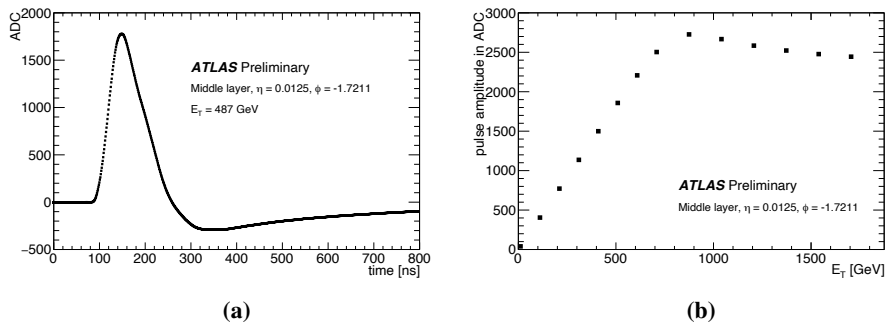
(a)   **(b)**

Figure 6: (a) Measured pulse shape of a SC in the EMB. The pulse is generated by injecting a predetermined amount of charge (DAC=4400) into the electrode of the calorimeter from the calibration board. The sampling phase relative to the pulse is determined by a stepped delay with interval of 1.04 ns selected on the calibration board. (b) Measured amplitude of calibration pulse (in transverse energy) as a function of injected amount of charge. The injected amount of charge is generated by a DAC at the calibration board, and the DAC setting is converted into a transverse energy based on test beam results. The amplitude of the pulse is measured by optimal filtering. [8]

remain operational with the same performances as at the end of Run-2, being proven to be stable and robust. The new digital trigger will be operated concurrently, and it has already proven to be able to reconstruct and digitize detector signals. An extensive campaign of calibrations is ongoing to cross check the various elements of the new system and to prepare it for the LHC pilot beam expected in October 2021 and for the first Run-3 collisions expected for March 2022.

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