PROCEEDINGS OF SCIENCE

Upgrade of the CSC Muon System for the CMS Detector at the HL-LHC

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The Large Hadron Collider (LHC) will be upgraded in several phases to expand its physics program significantly. After the current long shutdown from 2018-2021 (LS2) the accelerator luminosity will be increased to $2-3\times10^{34}$ cm^{-2}s^{-1} exceeding the design value of 1×10^{34} cm^{-2}s^{-1} allowing the CMS experiment to collect approximately 100 fb^{-1}/year. A subsequent upgrade in 2023-24 will increase the luminosity up to 7.5×10^{34} cm^{-2}s^{-1}. The CMS muon system must sustain a physics program after the LS2 shutdown that maintains sensitivity to electroweak scale physics and for TeV scale searches similar to what was achieved up to now For the Cathode Strip Chamber (CSC) muon detectors. The on chamber front-end readout electronics portion of the CSC electronics upgrade has now been completed. The design of the upgraded CSC electronics will be discussed, as well as the status of the commissioning of the upgraded CSC system. In view of the operating conditions at HL-LHC, it is vital to assess the detector performance for high luminosity. Accelerated aging tests are being performed to study the behaviour of the CSC detectors under conditions which are nearly an order of magnitude beyond the original design values. The status of this irradiation campaign and results will be presented.

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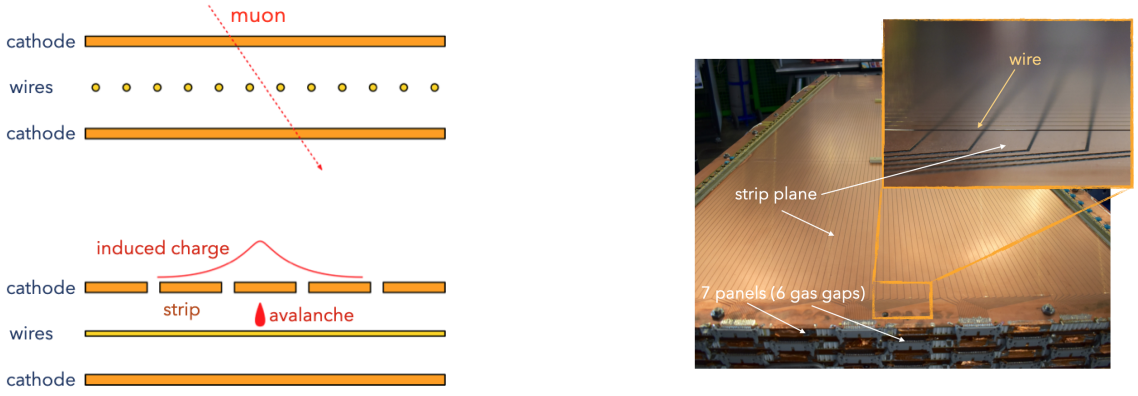
1. Introduction

The Compact Muon Solenoid (CMS) experiment [1] contains four muon detector subsystems as the Long Shutdown 2 (LS2) ends, each of which uses different variants of gaseous detection technology. In the forward region close to the beam-pipe, the Cathode Strip Chamber (CSC) system employ MultiWire Proportional Counters (MWPC) [2] with a finely segmented cathode strip readout, providing both tracking and triggering information in the absolute pseudo-rapidity range 0.9–2.4. Fig. 1a illustrates the operation of the cathode strip chambers.

The CSC system comprises 540 chambers in total divided between two endcaps; each endcap hosts four stations positioned along the z-axis of the CMS detector; each station has 2 to 3 rings of CSCs, where the ring planes are perpendicular to the beamline. The CSC chambers are labelled according to their location within the CMS detector. The convention states on which CMS endcap, station and ring a chamber resides; `ME±Station/Ring`. Each CSC chamber comprises six gas gaps with gold-plated tungsten wires sandwiched between two copper plates and filled with a gas mixture of 40% Ar, 50% CO_2 and 10% CF_4. Fig. 1b shows the wires and the strips inside a CSC chamber.



(a) **(b)**

Figure 1: The operation principle of a Cathode Strip Chamber when a charged particle passes through, 1a, and pictures 1b showing the inside of a CSC chamber.

The primary front-end electronics installed on each chamber are the Anode Front End Board (AFEB), the Anode Local Charged Track (ALCT) baseboard and mezzanine and the Cathode Front End Board (CFEB). In addition, the Low Voltage Distribution Board (LVDB) and Motherboard (LVMB) provide control and monitoring as well as powering the chamber front-end boards. AFEBs gathers signals from 16 wire groups, 8 per layer, and send them into the ALCT baseboard. The ALCT mezzanine hosts a Field Programmable Gate Array (FPGA) that determines the presence of charged particle tracks in the wire groups. The CFEB amplifies the cathode strips signal and quickly identifies potential ionization tracks using the onboard FPGA.

Moving outside the CMS detector, each set of 9 chambers, there is one VME crate containing off-chamber electronics, located approximately a dozen meters from the vicinity of the CMS detector. The Trigger Mother Board (TMB) receives triggering information from the ALCT and the Digital CFEB (DCFEB) boards to create Local Charged Track (LCT) candidates. Each LCT

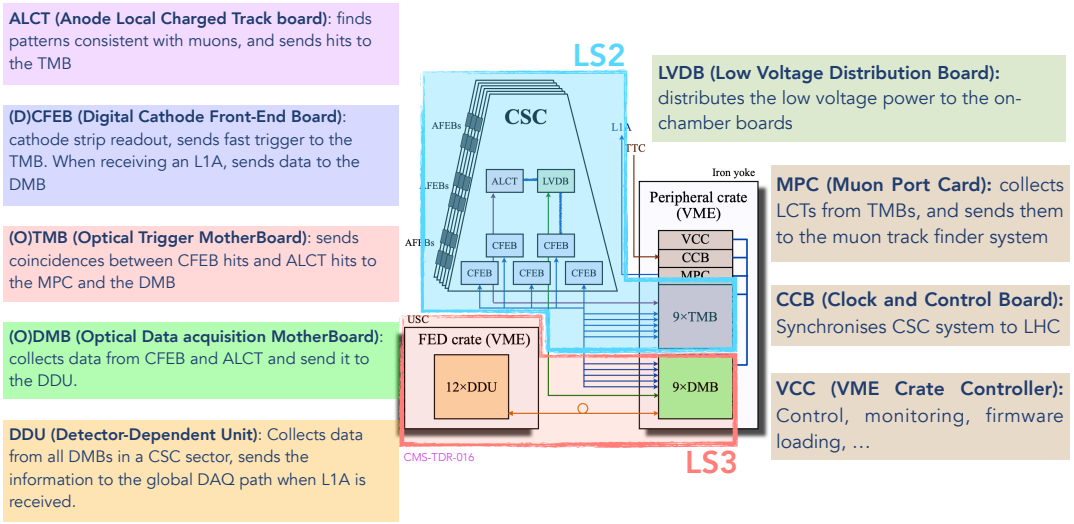


Figure 2: Layout of the on-chamber and off-chamber electronics. During LS2, the ALCTs, (D)CFEBs, and (O)TMBs are upgraded. During or before LS3, the (O)DMBs and FED system are upgraded. This figure is particular to non-ME1/1 chambers, with the principle differences being that ME1/1s have 7 Digital CFEBs and optical variants of the TMB and DMB

is formed from the coincidence with an anode local charged track and a cathode local charged track, the former contains information on the azimuthal position of track segment, the bend angle due to the magnetic field, and the pattern of cathode half-strips with hits in a chamber. When a coincidence is found between the wire groups and cathode strips, a signal is sent to the central triggering system to determine whether to initiate the event readout. The central triggering system then sends back a so-called Level-1 Accept (L1A) to the Data-Acquisition Mother Board (DMB) to readout from CFEBs and ALCT and transmit the data to the Front End Driver (FED). Every chamber has a dedicated pair of DMB and TMB boards. Every crate is equipped with a VME Crate Controller (VCC) that take care of control, monitoring and firmware loading; a Clock and Control Board (CCB), which synchronises the electronics to the LHC collisions; a Muon Port Card (MPC) that collects the LCTs from TMB and send them to the Endcap Muon Track-Finder. Fig. 2 shows a simplified schematic of the CSC electronics.

The High-Luminosity LHC (HL-LHC) project aims to increase the luminosity up to $7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$, with Level-1 trigger rates reaching 750 kHz with a latency of 12.5 μs [3] required by the tracker Level 1 Trigger subsystem that will be intruded in phase-II. Although the CSC modules are expected to provide satisfactory performance throughout the HL-LHC program [4], some electronics of the innermost chambers will need to be replaced in order to handle the harsh environment of HL-LHC to ensure stringent trigger requirements. In fact, longevity studies[5] using GIF++ facility as CERN in which CSC modules were irradiated to the equivalent of 10 years of HL-LHC data-taking anticipate good performance during Phase-2; however, the electronic readout system would suffer data losses, especially at high pseudo-rapidity due to increased chamber occupancy. New electronic boards will handle higher chamber occupancy rates, mainly with high-

speed optical links and more powerful processors.

2. The CSC Electronic Upgrade

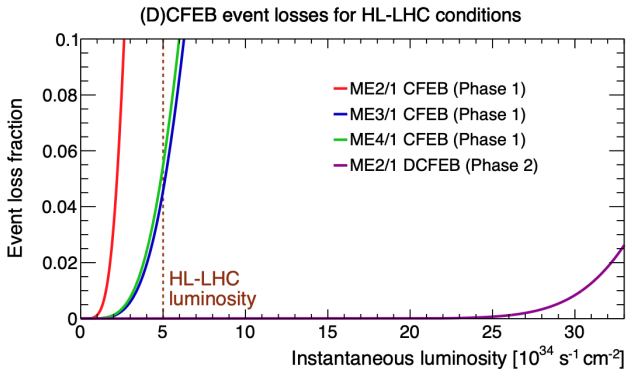


Figure 3: CFEB (Phase-1) and DCFEB (Phase-2) event loss fractions for HL-LHC conditions in the inner CSC rings ME2/1, ME3/1, and ME4/1 as a function of instantaneous luminosity. The design HL-LHC luminosity is marked by the dashed brown vertical line.

The increases to the trigger and particle rates mentioned above would result in large memory overflows, significant readout inefficiencies and event losses are expected. Fig. 3 shows the average event loss fraction for ME2/1, ME3/1 and ME4/1 stations as a function of the instantaneous luminosity. The CSC chambers closest to the beam-line require upgraded electronics, both on and off chambers. Due to schedule constraints of LS3, all the necessary on-detector replacement targeting phase-II has been already completed during LS2. Below is a list of the electronics that are or will be upgraded toward the phase-II LHC operation.

Digital Cathode Front End Board (DCFEB) is an updated version of the CFEB equipped with `Virtex-6` FPGA, fast 12-bit 20 MHz flash ADCs, and upgraded buffers. They are designed and installed as an upgrade for ME1/1 chambers during LS1. During LS2, these boards are replaced and passed down to the ME2/1, ME3/1, and ME4/1 chambers. The ME1/1 chambers are now instrumented with a new board xDCFEB (DCFEBv2) equipped with CERN's radiation-hard Versatile Twin Transmitter (VTTx) and bidirectional Versatile Transceiver (VTRx). This board includes a new capability to remotely program the FPGA via the optical link and Gigabit Transceiver (GBTx), providing a backup option in the event of EEPROM death due to the high radiation environment. Due to problems with the original optical transmitters on DCFEBs, they are retrofitted with VTTxs during the upgrade. Fig. 4 shows the differences between the DCFEB and DCFEBv2 boards.

Anode Local Charge Track Board (ALCT) mezzanines are equipped initially with `Virtex-E` FPGA, which has insufficient memory resources and output bandwidth to handle HL-LHC. The new mezzanines employ `Spartan-6` FPGA, with 9–12 times Block RAM comparing to its old counterpart. They include optical transmitters providing 8 to 12 times the bandwidth for the forward-most rings. For chambers that readout 288–382 wire-groups, a smaller Spartan-6 is used;

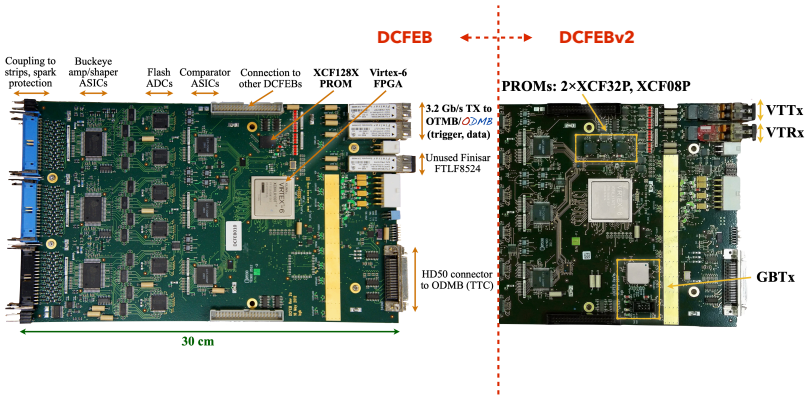


Figure 4: Top side of one of the DCFEBs produced for the ME1/1 upgrade compared to the updated version DCFEBv2.

the `ALCT-LX100` includes a VTRx that supports optical data readout to the new ODMB7 (4.48 Gbps) and EEPROM-less programming as in xDCFEB boards. For the larger chambers, an `ALCT-LX150T` is installed. A VTTx provides up to 6.4 Gbps data transmission to new ODMB5s. For the run3 operation, the copper interconnects will be used.

Optical Data-Acquisition Mother Board (ODMB) will replace, by the time of the HL-LHC operation, the current DMB boards. Two versions of ODMB7 and ODMB5 will be built, one for the ME1/1 chambers and another for the ME234/1 chambers. This board is based on the LS1 design but with more processing power. It will be based on the new `Xilinx 7` series family FPGA, with an output bandwidth up to 40 GB/s. A prototype is currently being tested at CERN.

Front-End Driver (FED) will also be upgraded. It will be based on the industry standard, the *Advanced Telecommunications Computing Architecture (ATCA)* and will be common to many CMS upgrade projects. It will deliver up to 600 GB/s of data to the CSC data acquisition system. The CSC subsystem will share the same processing module with parts of the newly installed GEM muon sub-detector. The shared module will consist of an APX Consortium card (called X2O) with 100 bidirectional links rated at 25 Gb/s and a `Virtex Ultrascale` FPGA. The total CSC data acquisition rate will reach 1344 Gb/s, an aggregate of chambers using DMB boards with 1.6 Gbps links, chambers equipped with ODMB5 using 2 to 3 links with 12.25 Gb/s, and 72 ME1/1 chambers using 4 links of 12.25 Gb/s per ODMB7. At a minimum, 9 X2O boards will make up the new FED system, replacing 36 Detector Dependent Unit (DDU) boards.

3. Additional Studies toward HL-LHC

The CSC electronic component will be exposed to intense radiation at the HL-LHC. Radiation-hard electronic components such as optical transceivers and EPROMs are needed, especially for the innermost rings. This will be done at various facilities; CHARM (CERN), TAMU and UC Davies cyclotrons and TAMU reactor. Each component will receive a dose up to 30 kRad equivalent to 3 times the projected dose of the HL-LHC.

Another area currently under study is the alternative gas mixtures, where alternatives to CF_4, used as an anti-ageing additive that prevents wire etching and polymerization, are explored. The European Union restricts the usage of greenhouse gases, including CF_4 that has a Global Warming Potential (GWP) above 7000 times the effect of CO_2 for 100 years. Two possible approaches are considered; 1) study the longevity of the chambers with a lower concentration of CF_4 or 2) explore more eco-friendly gases such as HFO (which has a GWP < 1 for 100 years). Preliminary studies [6] show similar gas gain and drift velocities as 10% CF_4 with a 100 V high-voltage working point shift. Further studies are scheduled for the end of 2021 at the GIF++ facility at CERN.

4. Conclusion

The CSC muon system that equips the CMS endcaps is being upgraded to handle the higher data rates of the HL-LHC. On-chamber electronics of the ME1/1 and ME234/1 chambers have been successfully upgraded on eight rings of the CSC muon system as of December 2020. Currently, the newly upgraded chambers are under commissioning, and preparation for LS3 has already started. Irradiation studies and alternative gas mixture studies are under preparation targeting LS3.

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