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Development and Performance of the Belle II DAQ Upgrade

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Belle II is a new-generation B-factory experiment operating at the luminosity frontier, SuperKEKB collider, and started data-taking in April 2018. Belle II uses a synchronous data acquisition (DAQ) system based on a pipelined trigger flow control. It is designed to handle 30 kHz trigger rate, under the assumption of a raw event size 1 MB. Because a larger event size and rate are foreseen depending on the future background conditions, and the difficult maintainability of the current readout system during the Belle II entire operation period is expected, we decided to upgrade the Belle II DAQ readout system with state-of-art technology. A PCI Express based new-generation of readout board (PCIe40), which was originally developed for the upgrade of LHCb and ALICE experiments, has been used for the upgrade of Belle II DAQ system. PCIe40 is able to connect to a maximum of 48 frontend electronics through multi-gigabit serial links. PCI Express hard IP-based direct memory access architecture, the newly designed timing and trigger distribution system and slow control system make the Belle II readout setup a compact system. Three out of seven sub-detectors of Belle II experiment have been operated with the upgraded DAQ system during physics data-taking, development and performance for remaining sub-detectors have been accomplished and checked with cosmic data-taking and stress DAQ test.

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1. Introduction

Belle II [1] is an experiment dedicated to exploring new physics beyond the SM in the flavor sector at the luminosity frontier. The SuperKEKB collider [2], located at KEK, Tsukuba, Japan, is designed based on the "nano-beam" scheme to achieve the instantaneous luminosity of $6.5 \times 10^{35}\ cm^{-2}s^{-1}$, which is approximately 35 times that of its predecessor KEKB, by colliding 7 GeV electrons and 4 GeV positrons. It can produce copious amounts of B and D mesons and τ leptons. The large statistics of data enables precise measurements of rare decays for testing SM with unprecedented sensitivity. The Belle II experiment aims to collect 50 ab^{-1} integrated luminosity by 2035.

The Belle II detector [1] is a general-purpose spectrometer upgraded or replaced with respect to the Belle detector. It is configured around a 1.5 T superconducting solenoid surrounding the interaction region. The Belle II detector consists of a vertex detector (VXD), central drift chamber (CDC), particle identification (PID) detector, electromagnetic calorimeter (ECL), and neutral K_L and Muon (KLM) detector, which are located from the inside to the outside of the detector. The VXD is made of a silicon pixel detector (PXD) and a silicon-strip vertex detector (SVD) used for detecting decay vertices. The CDC located outside the SVD is used as a tracking detector for precise measurement of momentum and energy loss of charged particles. Using the Cherenkov counter technique, the PID detector is divided into barrel and endcap (forward) parts, which are the time-of-propagation (TOP) counter and the proximity-focusing Aerogel Ring Imaging Cherenkov detector (ARICH), respectively. The ECL uses CsI(TI) crystals in the barrel and endcap regions. The KLM uses glass-electrode resistive plate chambers (RPCs) for the outer barrel region and layers of scintillator fibers for the endcap regions and the innermost layer of the barrel region.

2. Belle II DAQ and readout system

The Belle II DAQ [3] system is designed to process the data from the front-end electronics (FEE) to the storage system through several steps based on a highly unified system. As shown in Fig. 1, the highly unified timing and trigger distribution (TTD) system [4] first distributes Level 1 (L1) triggers to each FEE board. The digitized signals from the FEE boards of each sub-detector, except for the PXD, are read out by a unified readout system based on the common module called

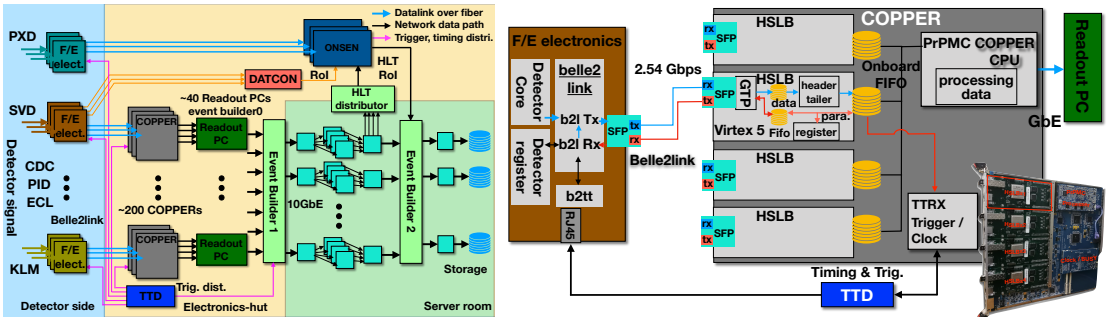

Figure 1: Block diagram of the Belle II DAQ system (left pad), and Schematic view of unified COPPER readout system.

Common Pipelined Platform for Electronics readout (COPPER) [5], as shown in right pad of Fig. 1. A total of 203 COPPERs are used in the original Belle II DAQ system before upgrade. To unify the readout system, a high-speed data transmission based on the custom serial link protocol, called Belle2link [6], is adopted. Xilinx GTP or GTX RocketIO up to 2.54 Gb/s, driven by the 127 MHz system clock, is used as the transceiver. As shown in right pad of Fig. 1, each COPPER module hosts four custom High Speed Link Boards (HSLB). The data formatting (per link) and module-level event building are processed by the on-board CPU on the COPPER module; subsequently, the data from several COPPER modules are collected to a readout PC through the Gigabit ethernet. The event building and software event selection are performed by high-level trigger (HLT) farms [7]. Finally, the selected data are sent to the storage servers.

3. PCIe40 based new Belle II readout system

The current readout system, mainly the COPPER module and its readout PC, is obstructing high-speed data transfer and DAQ maintenability. The number of disconnected parts are increasing, such as the chipset of PrPMC. In addition, the smallest bandwidth is in the Gigabit Ethernet between the COPPER module and the corresponding readout PC. PCIe40 [8] is a new generation of readout modules based on the PCI Express Gen3 solution with a high data throughput of 100 Gb/s [9]. The module will also be used for the DAQ upgrade of the LHCb and ALICE experiments at the Large Hadron Collider (LHC). PCIe40 fulfills the requirements of the Belle II DAQ upgrade and a large amount of data can be easily transferred from a readout board to a PC server via PCI Express bus. To integrate the current Belle II DAQ system, we particularly focus on the design of the firmware and software based on the PCIe40 board. Because all functionalities of the current readout system are retained, no modification of the firmware and hardware of the sub-detector FEE is required. A single PCIe40 board can connect up to 48 bidirectional optical links, while only 4 bidirectional links can be handled by the COPPER module. Thus, the new readout system will become much more compact by replacing 203 COPPERs with 21 PCIe40 boards (SVD: 5, CDC: 8, TOP: 2, ARICH: 2, ECL: 2, KLM: 1, TRG:1).

As illustrated in Fig. 2, four pairs of onboard MiniPOD optical transceivers are used to receive or transmit data from or to the FEE through optical fibers. A high-density Intel Altera Arria 10 field-programmable gate array (FPGA) chip (1.15 million cells) provides the board with powerful reconfigurable logic capabilities. PCIe40 is capable of running at up to 5 Gb/s for each link using

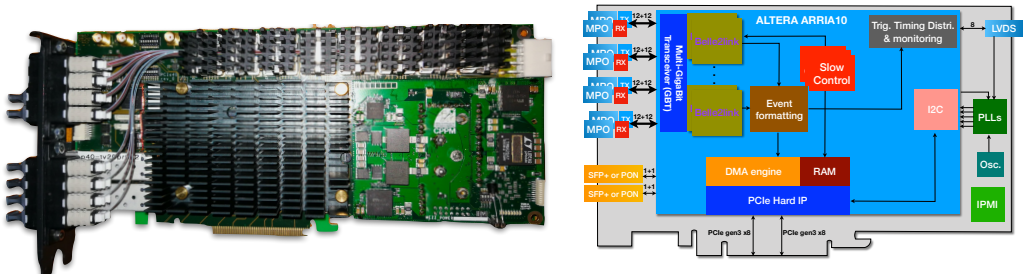

Figure 2: Photograph of PCIe40 module (left), and block diagram of the PCIe40 board illustrating the key features of the board.

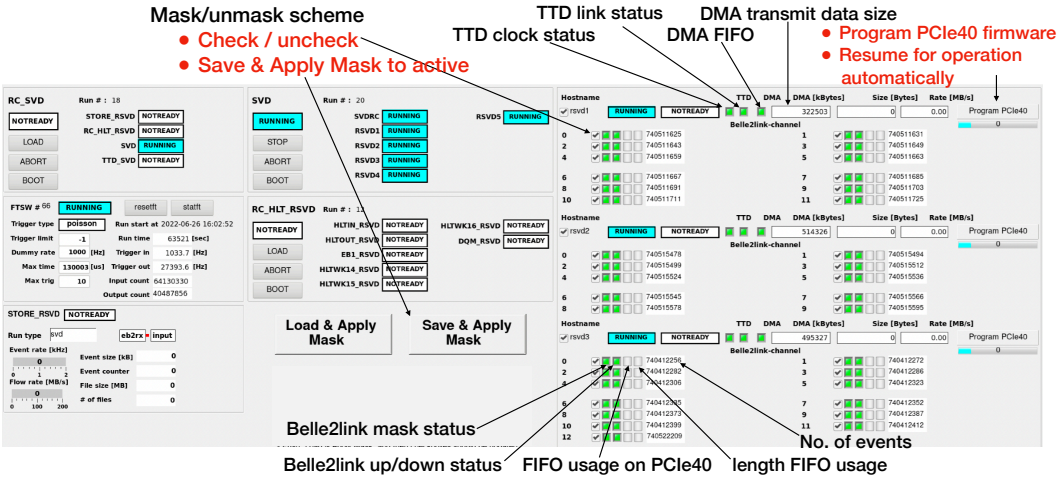

Figure 3: A unified control panel for sub-detector operations. The block of RC_SVD is used to control the run as a top level node, it controls the second level nodes, including TTD, readout PC, HLT, and STORE systems. Each readout PC (RSVD1...) control the corresponding PCIe40 module.

the Gigabit Transceiver (GBT) architecture with a maximum of 48 bidirectional links. A point-to-point PCI Express Gen3×16 links is used to connect the PC server and PCIe40 board. A PCIe40 board is presently installed in a 1U rackmount server (Xeon E5-2640v4 10Core/2.4GHz). Multiple PCIe40 boards can be installed in a larger server. Belle2link protocol, b2tt protocol, and slow control functionalities which are implemented in the current COPPER-HSLB system, need to be integrated to the PCIe40 system. Event formatting and event building, as well as PCI Express hard IP-based direct memory access (DMA) are newly designed for PCIe40. Ref. [10] has more detailed description about the firmware and software development for Belle II DAQ upgrade.

A unified control panel was developed for operating the PCIe40 based DAQ system, panel for SVD is shown in Fig. 3 as an example. It is used to control the run, monitor the running status of each node, as well as investigate and debug the cause of errors occurring in the DAQ system. There are also functions developed for masking a specific front-end electronics, programming the PCIe40 firmware and resuming the operation automatically. Meanwhile, run status, status of each node, PCIe40 status, and the error information are saved into the logging system so that it can be easily integrated into the current Belle II logging and monitoring system.

4. Performance of new readout system

The performance of PCIe40 based readout system have been tested on the test bench, and the Belle II DAQ system. As shown on the left and middle pads of Fig. 4, the optical fibers from front-end electronics are connected to the patch panels, and then bundled into MPO fibers and connected to PCIe40 module, which is installed in the readout PC shown in the middle pad of Fig. 4. PCI Express hard IP-based DMA architecture of the new readout hardware is capable of handling a 260-kHz trigger rate with 17 Gb/s data throughput without data loss, and the maximum data transfer rate can reach to 31 Gb/s [10]. The current performance of the data readout system

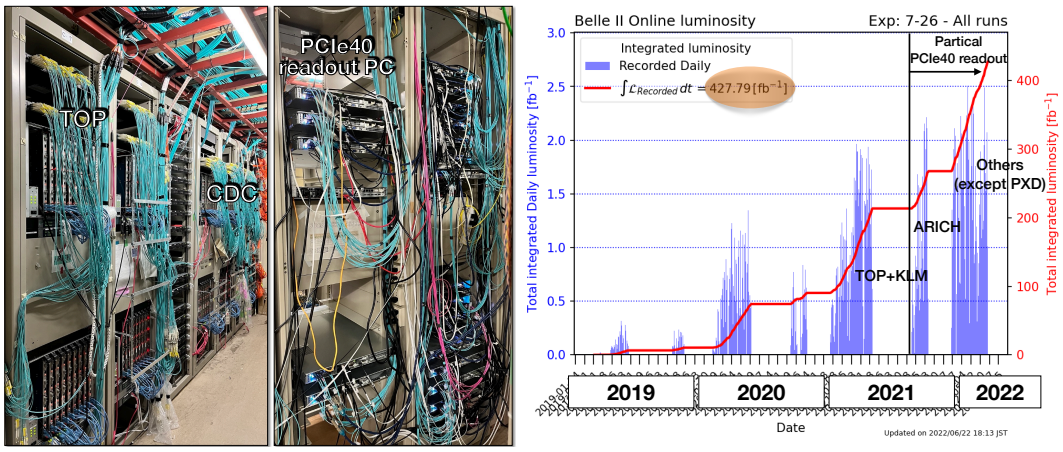

Figure 4: Photograph of installed PCIe40 readout system (left and middle pad), and integrated luminosity of Belle II experiment (right pad).

already fulfils the Belle II DAQ upgrade requirements, while the throughput limit of the new readout system is 10 Gb/s, which is determined by the NIC of new readout PC.

A test of remote access to the registers in the front-end electronics through Belle2link was performed together with data acquisition under different trigger rates. The register access rates for the COPPER-HSLB system decreased from 170 to 0 accesses / sec, when the data acquisition trigger rate increased from 0 to 30 kHz. This indicates that there was a limitation of bandwidth of the COPPER-HSLB system for slow control and data acquisition. However, the corresponding register accessing rates for the PCIe40 board retained a constant value even when the data acquisition trigger rate was increasing. There was no limitation of bandwidth observed for the PCIe40 board [10].

Right pad of fig. 4 shows the integrated total (red) and daily (blue) luminosity from April 2019 to June 2022. TOP and KLM readout systems were firstly replaced by the PCIe40 module for physics data-taking from autumn run of 2021, then ARICH started using PCIe40 readout system from Spring run of 2022. The data-taking efficiency of Belle II experiment kept around 90% before and after replacement of COPPER to PCIe40 readout system. The partial upgrade of Belle II DAQ system has been confirmed to be successful.

5. Commissioning of full PCIe40 based Belle II DAQ system

Installation and development for the replacement of SVD, CDC, ECL and TRG systems have been performed. As shown on the left pad of Fig. 5, stress DAQ test running with 30 kHz Poisson-distributed random dummy trigger configuration has been performed to confirm the performance for the remaining systems. It has been confirmed that the system could continue running for about 8 hours without error. Meanwhile, cosmic-ray runs were taken with both COPPER and PCIe40 based readout systems. These cosmic-ray runs can be used to check the quality of data readout by the PCIe40 system. For instance, right top pad of Fig. 5 shows an estimator, the cluster charge of SVD, read out by COPPER system, and the right bottom pad shows the same estimator read out by PCIe40 system. We have also checked other monitoring variables and confirmed no significant differences between the COPPER and PCIe40 based readout systems can be found. The PCIe40

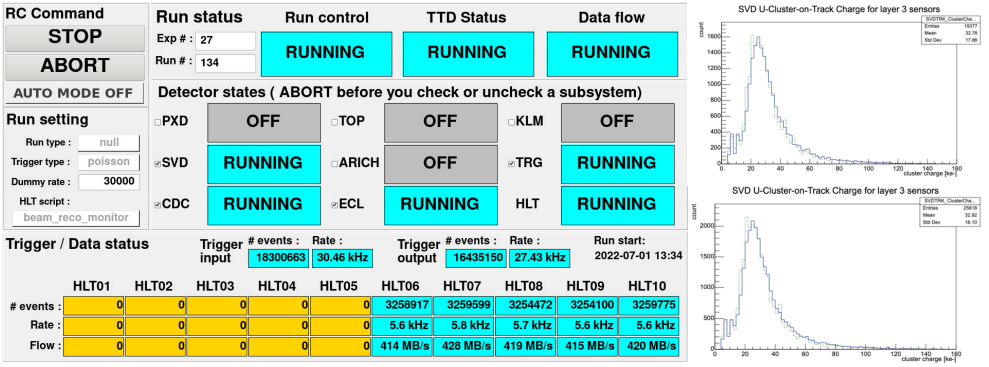

Figure 5: Global operation panel during the commissioning with SVD, CDC, ECL and TRG sub-systems for a stress DAQ test (left pad). A data quality estimator, cluster charge, of SVD detector readout by the COPPER (right top pad) and PCIe40 (right bottom pad) system during a dedicated cosmic-ray run.

based DAQ system will be fully operated for physics data-taking from next run period starting in autumn 2023.

References

[1] T. Abe, et al., "Belle II Technical Design Report," *arXiv:1011.0352*, Nov. 2010.

[2] K. Akai, K. Furukawa, H. Koiso et al. (SuperKEKB Collaboration), "SuperKEKB collider," *Nucl. Instrum. Methods Phys. Res., Sect. A* vol. 907, pp. 188-199, Nov. 2018.

[3] S. Yamada et al., "Data acquisition system for the Belle II experiment," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 1175-1180, Jun. 2015.

[4] M. Nakao, "Timing distribution for the Belle II data acquisition system, " *J. Instrum.*, vol. 7, no. C01028, Jan. 2012.

[5] T. Higuchi et al., "Modular pipeline readout electronics for the super-belle drift chamber," *IEEE Trans. Nucl. Sci.*, vol. 52, pp. 1912-1917, Oct. 2005.

[6] D.Sun et al.,"Belle2Link:A global data readout and transmission for Belle II experiment at KEK," *Phys. Procedia*, vol. 37, pp. 1933-1939, 2012.

[7] R. Itoh et al., "Data flow and high level trigger of Belle II DAQ system," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 3720-3724, Oct. 2013.

[8] J. P. Cachemiche, "The PCIe-based readout system for the LHCb experiment," *Topical Workshop on Elect. for Part. Phys.*, Lisbon, Portugal, Sep. 2015, 10.1088/1748-0211/11/02/P02013.

[9] P. Durante, N. Neufeld, R. Schwemmer, U. Marconi, G. Balbi and I. Lax, "100Gbps PCI Express readout for the LHCb upgrade," *2014 19th IEEE-NPSS Real Time Conference*, Nara, 2014, pp. 1-3, doi: 10.1109/RTC.2014.7097492.

[10] Q. D. Zhou et al., "PCI Express based high-speed readout for the Belle II DAQ upgrade" *IEEE Trans. Nucl. Sci.*, vol. 68, no. 8, pp. 1818-1825, Aug. 2021.