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The CMS ECAL upgrade for precision timing measurements at the High-Luminosity LHC

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The High Luminosity upgrade of the LHC (HL-LHC) at CERN will provide unprecedented instantaneous and integrated luminosities of around 5 x 10^{34} cm^{-2} s^{-1} and 3000 fb^{-1}, respectively. An average of 140 to 200 collisions per bunch-crossing (pileup) is expected. In the barrel region of the Compact Muon Solenoid (CMS) electromagnetic calorimeter (ECAL), the lead tungstate crystals and avalanche photodiodes (APDs) will continue to perform well, while the entire readout and trigger electronics will be replaced. The noise increase in the APDs, due to radiation-induced dark current, will be mitigated by reducing the ECAL operating temperature. The trigger decision will be moved off-detector and performed by powerful and flexible FPGA processors.

The upgraded ECAL will greatly improve the time resolution for photons and electrons with energies above 10 GeV. Together with the introduction of a new timing detector designed to perform measurements with a resolution of a few tens of picoseconds for minimum ionizing particles, the CMS detector will be able to precisely reconstruct the primary interaction vertex under the described pileup conditions.

We present the status of the ECAL barrel upgrade, including time resolution results from beam tests conducted during 2018 and 2021 at the CERN SPS.

41st International Conference on High Energy physics - ICHEP2022
6-13 July, 2022
Bologna, Italy

PoS(ICHEP2022)642

1. Introduction

The electromagnetic calorimeter (ECAL) plays a key role in the detection of electrons and photons for the CMS experiment at LHC. It is composed of a barrel (EB), covering the central rapidity region (up to $|\eta| = 1.48$) and two endcaps (EE), which detect incident particles up to $|\eta| = 3.0$. It was designed to achieve an excellent photon and electron energy resolution, particularly for the search of a Higgs boson in the two-photon decay channel and subsequent precision measurement of its properties, but also in the four-lepton channel decay and other research topics within and beyond the Standard Model.

While very successfull at meeting the design requirements and contributing prominently to the CMS physics program, ECAL was designed to maintain this level of performance up to an integrated luminosity of 500 fb^{-1}. At the end of the HL-LHC program an integrated luminosity of 4500 fb^{-1} will be accumulated in a harsher environment: this requires an upgrade of the EB readout electronics, discussed in the following, while the transparency loss in EE will be large enough to require its replacement with a completely new detector [1].

2. The CMS ECAL detector

The CMS ECAL is a homogeneous calorimeter made of 75848 lead tungstate ($PbWO_4$) scintillating crystals, located inside the CMS superconducting solenoid magnet. The photodetectors are avalanche photo-diodes (APD) in the barrel and vacuum phototriodes (VPT) in the endcaps. The barrel region is made of 36 identical supermodules (SM), each containing the crystals, APDs, and readout electronics. The latter includes very front-end (VFE) cards, which provide pulse amplification, shaping, and digitisation functions, and front-end (FE) cards which provide data pipeline, data transmission, and trigger primitive formation functions. A passive distribution card, the Motherboard, connects the APDs to the VFEs. Electrons and photons are typically reconstructed up to $|\eta| < 2.5$, the region covered by the tracker, while jets are reconstructed up to $|\eta| = 3.0$. The ECAL energy resolution achieved during 2010 and 2011 ranges from 1.1 to 2.6% in the barrel and 2.2 to 5% in the endcaps for photons from Higgs boson decays.

3. The ECAL upgrade for HL-LHC

The main challenges that the ECAL detector will have to face during the HL-LHC program are radiation-induced degradation effects and more demanding data-taking conditions. The first will cause a loss of crystal transparency and an increase in the APD leakage current and therefore noise. To mitigate the increase in APD leakage current, the operating temperature will be reduced from the current 18°C to 9°C. As for the data-taking conditions at HL-LHC, the concurrent number of proton-proton interactions is foreseen to increase from the current 40 to up to 200. In order to identify the primary interaction vertex from the other vertices in the same bunch crossing, a more precise time resolution, better than 30 ps for showers above 50 GeV, will be needed. To meet this goal, a faster front-end electronics was designed. This improvement will also result in better discriminating power between scintillation light generated by electromagnetic showers from the faster anomalous signals caused by particles hitting the APD directly. The back-end, off-detector

electronics is also being redesigned, in order to obtain greater flexibility in the trigger and comply with the increased CMS-wide level-1 (L1) trigger latency (from 3.5 μs to 12 μs) and rates (from 100 kHz to 750 kHz) [3].

4. The upgraded ECAL front-end electronics

For the HL-LHC phase, the scintillating crystals, the APDs and the Motherboards will be kept in place, while the VFE, FE, and back-end electronics have been completely redesigned. The APD output will be sampled and each sample shipped out to the off-detector electronics using high-speed optical links. The front-end will comprise a new, faster analog electronics and the sampling rate will increase from 40 to 160 MHz, with 12-bit resolution, to obtain better time resolution and anomalous signal discrimination. The cost of this improvement is the increase in data rate, for which a loss-less data compression mechanism was devised.

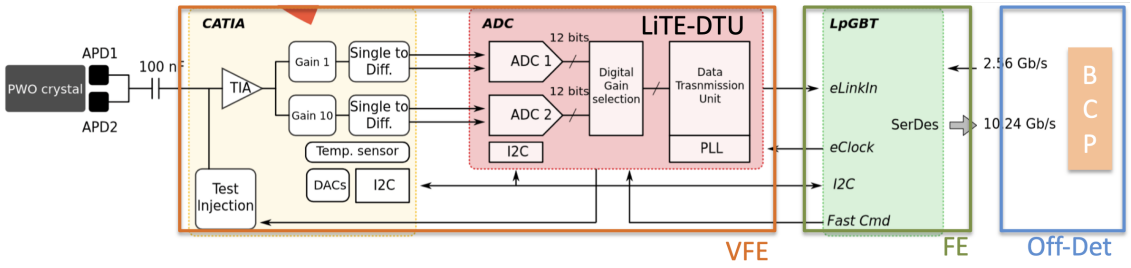

Figure 1: Block representation of the EB readout electronics for HL-LHC

Figure 1 shows a block diagram of the new readout electronics. The upgraded VFE comprises an analog ASIC called CATIA, which implements two transimpedance amplifiers (TIAs) with 35 MHz bandwidth, and a digital ASIC called LiTE-DTU, comprising two 12-bit ADCs sampling at 160 MHz, data transmission with gain selection and compression. Each VFE reads five APDs and carries five channels, each channel consisting of a CATIA and a LiTE-DTU ASIC. Five VFEs are connected to a single FE card that collects data from the VFEs and transmits to the off-detector electronics using the lpGBT [4] optical transmission system. Also connected to the FE is a low voltage regulator board (LVR), a radiation-hard voltage regulator card based on the bPOL12 DC-DC converter [5]. Off-detector, the Barrel Calorimeter Processor (BCP) card will use high-end FPGAs to form the L1 trigger decision and read out the detector.

The CATIA ASIC is built in 130 nm CMOS technology. It comprises a high-gain (10x) and a low-gain (1x) amplification channel of the APD output, to cope with the dynamic range requirements, and it features test pulse injection, DC level adjustment and the ability to provide calibration levels to the ADC. The performances of the CATIA prototype have been tested in test beam campaigns and shown to be very good in term of noise, linearity, and time resolution. As an example, the integral non-linearity measured as a function of the amplitude of an injected test pulse is shown in Fig. 2 (left).

The LiTE-DTU ASIC is built in 65 nm CMOS technology. It includes two 12-bit ADCs running at 160 MHz, designed by a commercial company and specified for a ENOB (equivalent number of bits) of better than 10.2 at 50 MHz. The data transmission unit selects the highest

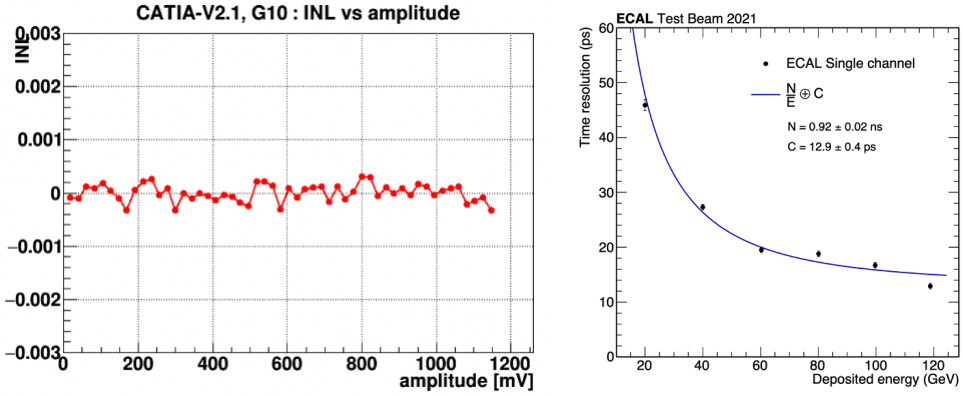

Figure 2: Left: Integral non-linearity of the CATIA amplifier in the high-gain channel. Right: Time resolution of a single channel obtained with an electron beam.

non-saturated gain channel and takes care of data transmission and compression. It includes a Phase-Locked Loop (PLL) circuit for clock generation, it is designed to be TID (total irradiation dose) tolerant up to 20 kGy and it features Single-Event Upset (SEU) tolerant logic. The lossless data compression mechanism exploits the fact that the spectrum of the hits in each ECAL crystal falls very rapidly with energy. The signal is above 2.5 GeV only in a small fraction of events. The compression algorithm was designed to use 6 bits to encode signals below 2.5 GeV, and 12 bits for signals above 2.5 GeV. This allows the reduction of the expected bandwidth occupancy to 1.08 Gb/s per channel, to be compared with the 2.08 Gb/s needed in absence of compression. The first prototype of the LiTE-DTU chip was under test in late 2019, while the latest, near-production iteration was performed in early 2022. The performance of the system in terms of time resolution is illustrated in Fig. 2 (right). The target resolution of 30 ps for energies above 50 GeV is achieved.

The function of the FE card is the streaming of digitized data generated on the VFE to the CMS ECAL back-end electronics, system initialization and control of all VFE components, and low-jitter distribution of the clock to VFE cards. It includes four lpGBT uplinks at 10.24 Gb/s and one downlink at 2.56 Gb/s. A final prototype is currently being tested with the front-end card prototypes. The LVR card provides regulated DC power supply to FE and VFE using the bPOL12 radiation-tolerant chip.

The off-detector BCP card will be common for ECAL and HCAL, the barrel section of the hadron calorimeter. Its purpose is trigger primitive generation, clock distribution, control, and data readout. It is implemented as an ATCA blade and the V1.0 prototype is based on the Xilinx Kintex Ultrascale KU115 FPGA. The BCP carries a large number of high-speed interfaces to the front-end, the CMS data acquisition, the LHC signaling system, and the neighboring BCPs.

5. Summary

The challenging conditions of HL-LHC, with a 4-5 fold increase in occupancy with respect to LHC, require a complete overhaul of the CMS electromagnetic calorimeter electronics. The readout chain has been completely redesigned, while keeping the crystals and photosensors. The bandwidth of the analog readout has been increased by a factor four, as well as the sampling

frequency. The trigger hardware was moved off-detector for maximum flexibility. The prototype ASICs and readout boards show excellent performances. At present a vertical integration test, to measure the performance of the readout chain end-to-end, is underway. A larger scale test, with the electronics effectively mounted on a ECAL module, is in preparation. Mass production is foreseen to begin in 2023.

References

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PoS(ICHEP2022)642