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The CMS MTD Endcap Timing Layer: Precision Timing with Low Gain Avalanche Detectors

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The Compact Muon Solenoid (CMS) detector at the CERN Large Hadron Collider (LHC) is undergoing an extensive upgrade program to prepare for the challenging conditions of the High-Luminosity LHC (HL-LHC). A new timing detector in CMS will measure minimum ionizing particles (MIPs) with a time resolution of ~40–50 ps per hit and coverage up to $|\eta|$=3. The precision time information from this MIP Timing Detector (MTD) will reduce the effects of the high levels of pileup expected at the HL-LHC and will bring new and unique capabilities to the CMS detector. The endcap region of the MTD, called the endcap timing layer (ETL), must endure high fluences, motivating the use of thin, radiation tolerant silicon sensors with fast charge collection. As such, the ETL will be instrumented with silicon low-gain avalanche diodes (LGADs), covering the high-radiation pseudo-rapidity region $1.6 < |\eta| < 3.0$. The LGADs will be read out with the ETROC readout chip, which is being designed for precision timing measurements. We will present the extensive developments and progress made for the ETL detector, from sensors to readout electronics, mechanical design, and plans for system testing. In addition, we will present test beam results, which demonstrate the desired time resolution.

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1. The CMS MTD Endcap Timing Layer at High Luminosity LHC

High-Luminosity LHC (HL-LHC) [1] will be the upgrade of the present LHC, and it will start operating in 2029. The instantaneous luminosity at HL-LHC will increase by at least a factor of ∼ 5, raising the number of proton-proton collisions in each bunch crossing from ~40 to 140–200. This high pile-up environment will cause difficulties in object reconstruction and particle identification due to tracks coming from nearby vertices. The addition of timing information is thus needed to separate those events overlapped in space but happening at different moments in time. For this reason, the Compact Muon Solenoid (CMS) Collaboration [2] has planned the design and construction of a new timing detector, the so-called Minimum Ionizing Particles (MIP) Timing Detector [3]. MTD will be a timing layer providing 4D tracking by associating timing information to the reconstructed tracks thanks to its excellent time resolution. The CMS MIP Timing Detector (MTD) will be composed of two sections: (i) the Barrel Timing Layer (BTL), equipped with LYSO crystals read-out by SiPMs, with a total surface of 38 m^2 and hermetic coverage for $|\eta| < 1.45$, and (ii) the Endcap Timing Layer (ETL), instrumented with 14 m^2 of Low-Gain Avalanche Diodes (LGADs) with a dedicated ASIC readout, covering the pseudorapidity region $1.6 < |\eta| < 3.0$. The choice of different technologies for the two regions takes into account the radiation levels and the area to be covered with sensors. The Endcap Timing Layer will have to withstand radiation fluences up to 1.7E15 n_{eq}/cm^2 by the end of its lifetime, and silicon sensors are the most suitable detectors to cope with such an environment. On the other hand, covering the 38 m^2 area of the barrel with silicon would be too expensive, and crystals represented the best compromise to instrument BTL. MTD will improve the event reconstruction by collecting timing information of the charged particles and combining tracking with timing to assign time information to each reconstructed vertex and track. This will be possible thanks to a timing resolution of σ_t ~30–40 ps at the start of HL-LHC, which will slightly worsen at the end of lifetime, when the resolution in the barrel region will degrade to σ_t ~50-60 ps due to radiation, while the degradation in the endcaps will be minimal. With these features, MTD will mitigate the pile-up effect from HL-LHC and contribute to maintaining the present CMS performances on background rejection.

Focusing on the endcap region, the ETL will be placed on the nose of the future High Granularity Calorimeter. It will include two disks for each endcap, covered in silicon sensors on both sides. As previously mentioned, its design provides hermetic coverage for the pseudorapidity range $1.6 < |\eta| < 3.0$. In addition, it ensures that 80% of tracks will cross two layers of silicon, granting that ETL will be able to provide a track timing resolution of σ_t<35 ps. The total track resolution is, in fact, the result of the squared sum of the single-hit timing resolution $\sigma_{singlehit}$ in the two ETL layers, where $\sigma_{single\ hit} = \sqrt{\sigma^2_{sensor} + \sigma^2_{readout}}$ <50 ps, with both σ_{sensor} and $\sigma_{readout}$ lower than 40 ps. ETL requirements are:

- a fill factor (ratio between active and total detector area) >95% for each layer, ensuring two timing measurements for a very high fraction of tracks;
- low occupancy, <0.1% at low η and ~1% at highest η, to avoid double hits and ambiguous time assignment;
- radiation tolerance up to a fluence of 1.7E15 n_{eq}/cm^2 in the inner region. A large part of ETL

will be exposed to less than 1E15 n_{eq}/cm^2, and only ~12% of its surface will reach higher fluences. To cope with radiation effects, ETL will be operated at a temperature below -25°C;

- a design allowing to access the detector for maintenance, where ETL can be placed in an independent volume, isolated, and operated separately from HGCAL.

2. The sensors for the CMS Endcap Timing Layer

The Endcap Timing Layer will be instrumented with silicon sensors based on the Low-Gain Avalanche Diode technology (LGAD) and optimized for precise timing measurements. LGAD sensors are n-in-p silicon diodes whose design provides moderate internal gain. Unlike traditional silicon diodes, they feature a gain layer, which is a highly-doped thin implant near the p-n junction. This layer causes the formation of a high local electric field, producing the multiplication of primary charges, at the basis of the gain mechanism. The gain factor must be moderate, between 10 and 30, to prevent multiplication noise from being dominant, and to consequently maximize the signal-to-noise ratio.
The requirements for the ETL sensors are the following:

- high yield for large multi-pad arrays,
- a very good gain uniformity,
- fill factor (ratio between active and total detector area) >95%,
- low leakage current to limit power consumption and noise,
- radiation resistance up to 1.7E15 n_{eq}/cm^2
- a uniform response with large signals delivering a charge >8 fC when new and >5 fC until the end of HL-LHC operation,
- a design fulfilling electronics needs while allowing low occupancy.

The final sensor for ETL will be a ~50 μm-thick 16×16 pad array with 1.3×1.3 mm^2 pads. After the R&D campaigns, prototyping studies are now ongoing to define the last details for the final ETL sensor design. Large-size prototypes have been produced by different vendors: Hamamatsu Photonics (HPK), Fondazione Bruno Kessler (FBK), Centro Nacional de Microelectronica (CNM), Micron Semiconductor, the Institute of High Energy Physics Chinese Academy of Science together with the Institute of Microelectronics of the Chinese Academy of Sciences (IHEP-IME), and Teledyne [4]. A Market Survey is now in progress for the selection of those vendors capable to provide suitable sensors for ETL.
Studies of production uniformity have been performed on wafer at the foundries. Vendors characterized each wafer in a production by performing IV and CV measurements on each structure. Their data have been used to compute the distribution of (i) breakdown voltage for every pad, (ii) leakage current at a fixed bias of every single pad, and (iii) depletion voltage of each pad. The results show that the latest LGAD productions have a high yield and low leakage current: in particular, the yield for 16×16 arrays is good, >70%. The gain layer doping disuniformity, representative of the sensor

response disuniformity, is <1%.
Timing resolution measurements have been performed in Torino [5] and at Fermilab, [6] with Beta-source setups based on Sr90 sources. As the sensors' performances have been benchmarked using very fast low-noise electronics, results might be different when reading out the LGADs with the ETL ASIC. The most performing prototypes can reach a timing resolution <40 ps up to fluences of 2.5E15 n_{eq}/cm^2 (Figure 1).

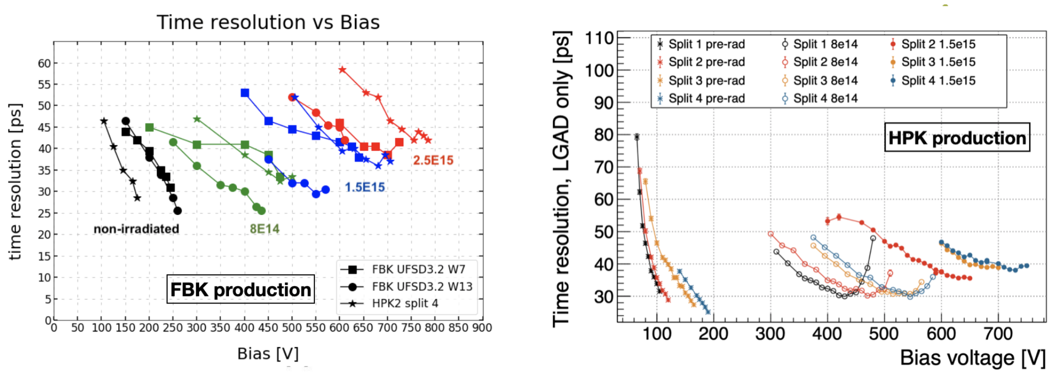

Figure 1: Timing resolution results pre- and post-irradiation for prototypes from FBK (left) and HPK (right) latest productions.

ETL prototypes have also been tested on a 120 GeV/c proton beam at the Fermilab test beam facility. The facility provides a setup instrumented with a strips and pixels telescope for precise tracking, a Photek MCP with 10 ps timing resolution used as a time reference, an independent scintillator providing the trigger, and an environmental test chamber hosting the LGADs under test. This configuration allowed the study of a limited number of sensors with high precision. Timing resolution maps have been obtained for both 2×2 and 5×5 devices when new demonstrating a uniform ~30 ps resolution. Uniform hit efficiency has been observed in large arrays as well, reaching ~ 100% in new sensors and ~ 99% after irradiation at a fluence of 8E14 n_{eq}/cm^2. These results prove that LGADs are highly uniform and efficient, able to reach target resolution on large multi-pad arrays [7].

3. ETROC, the ETL read-out ASIC

The ETL sensors will be read out by a dedicated ASIC, the Endcap Timing Layer Read-Out Chip (ETROC) [9]. It is designed to feature low noise and fast rise time while consuming a reduced power budget (1 W/chip, 3 mW/channel). These properties allow ETL to reach the target time resolution per single hit $\sigma_{singlehit}$<50 ps, thanks to a σ_{jitter}<40 ps. Four prototype versions of ETROC have been planned up to now [8]:

- ETROC0, a single analog channel;
- ETROC1, a full front-end with TDC and 4×4 clock tree. The chip is based on ETROC0 front-end with the addition of a TDC featuring a brand new design optimized for low power (~0.1 mW/pixel), achieved using simple delay cells with self-calibration;

- ETROC2, a full-size 16×16 ASIC with full functionality, submitted in October 2022;
- ETROC3, the pre-production chip, whose submission is foreseen in March 2024.

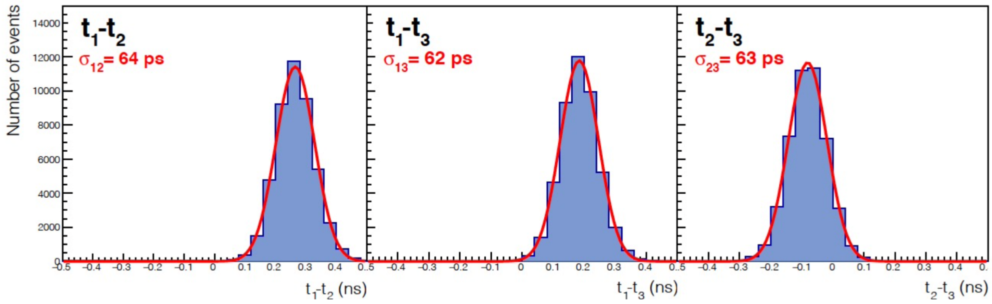

Figure 2: Distributions of time differences between pairs of ETROC1+LGAD layers from the three-layered telescope used at FNAL test beam, resulting in σ_{ij}=42–46 ps

ETROC0 and 1 have been already produced and tested. In particular, ETROC1 performances brought promising results in terms of resolution. The TDC resolution has been measured to be ~6 ps. Furthermore, timing resolution measurements have been performed at the Fermilab test beam facility. A beam telescope provided with three ETROC1+LGAD layers has been used to show the timing resolution achievable with large signals. Figure 2 displays distributions of time differences between pairs of telescope layers, where $\sigma_{t_i t_j} = \sqrt{\sigma_{t_i}^2 + \sigma_{t_j}^2}$: as a result, the total time resolution per hit reached for each LGAD+ETROC1 layer is σ_{t_i} ~42–46 ps.

4. The ETL modules

A strong effort was made to combine the inputs from the studies on the Endcap Timing Layer into the complete detector design and layout. To instrument the two ETL endcaps, containing 2 disks each with both their front and back faces instrumented, ~8000 sensor modules each will be needed [10]. These modules, together with the front-end electronics, need to fit in a very tight mechanical envelope: the total volume allocated for the ETL detector in each endcap, including the layers for supports and services, is 79 mm.
In the so-called TAMALES module layout, ETL modules are made of 4 16×16 pad LGAD sensors, bump bonded to one ETROC each. Sensors are in thermal contact with the cooling through an AlN baseplate, on which the devices are stuck. A multi-module readout board sits above the sensor modules and is directly wire-bonded to the PCB modules. The readout board is based on the CERN's radiation-hard Low Power Gigabit Transceiver (lpGBT) and Optical Link Module VTRx+. A first prototype provided with the full ETL readout chain, Prototype v1, has been developed in realistic for factor and successfully tested with an ETROC2 emulator [11].

5. Conclusions

The CMS Endcap Timing Layer will perform precise timing measurements of charged particles with single-hit timing resolution <50 ps, allowing the CMS detector to maintain its excellent

performance in the very challenging environment of the HL-LHC. ETL will be instrumented with thin Low-Gain Avalanche Diodes read out by the dedicated ETROC ASIC.
The latest LGAD productions have been measured both in laboratory and at test beam to ensure they meet all the required specifications. It has been observed that sensors have high yield and uniformity, a timing resolution <40 ps up to the end of ETL lifetime, and 100% efficiency and uniform time resolution across the whole active area of large LGAD multi-pad arrays at test beams.
The Endcap Timing Layer Read-Out Chip is required to provide excellent timing performances while exploiting a low power budget (3 mW/channel). ETROC1 can reach a timing resolution of 42–46 ps when coupled to an LGAD, as measured at the FNAL test beam. ETROC2 has been submitted in October 2022, while ETROC3 design is in progress and its submission is planned for March 2024.
LGADs and ETROC chips will be the main components of the ETL modules. A sensor module will include 4 LGAD sensors, bonded to an ETROC each, and provided with a dedicated readout board. The first prototype with a realistic form factor has been tested with the full readout chain.

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