PROCEEDINGS OF SCIENCE

Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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A new era of hadron collisions will start around 2029 with the High-Luminosity LHC, that will allow to collect ten times more data than what has been collected so far. This is possible thanks to the expected higher instantaneous luminosity and higher number of collisions per bunch crossing. To meet the new trigger and data acquisition requirements and to withstand the high expected radiation doses at the High-Luminosity LHC, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded. The triangular calorimeter signals will be amplified and shaped by analogue electronics over a dynamic range of 16 bits, with low noise and excellent linearity. Developments of low-power preamplifiers and shapers to meet these requirements are ongoing in 130 nm CMOS technology. In order to digitize the analogue signals on two gains after shaping, a radiation-hard, low-power 40 MHz 14-bit ADCs is being developed using a pipeline+SAR architecture in 65 nm CMOS. The characterization of the prototypes of these on-detector components is promising and likely will fulfill all the requirements. The signals will be sent at 40 MHz to the off-detector electronics, where FPGAs connected through high-speed links will perform energy and time reconstruction through the application of corrections and digital filtering. Reduced data will be then sent with low latency to the level-0 trigger-system, while the full data will be buffered until the reception of the trigger decision signal. For a triggered event, the full data will be sent to the ATLAS readout system. The data-processing, control, and timing functions will be realized with dedicated boards using the ATCA technology. Here, the results of tests of prototypes of the on-detector components will be presented. The design of the off-detector boards along with the performance of the first prototypes will be discussed. In addition, the architecture of the firmware and processing algorithms will be shown.

41st International Conference on High Energy physics - ICHEP2022
6-13 July, 2022
Bologna, Italy

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PoS(ICHEP2022)668

1. Introduction

The focus of these proceedings is the planned upgrades to the readout electronics of the ATLAS Liquid Argon (LAr) calorimeter for the High-Luminosity Large Hadron Collider (HL-LHC) era [1], which is expected now to begin in 2029. In addition to plans, the current state of progress in testing and development of prototypes is addressed.

The ATLAS LAr calorimeter is a sampling calorimeter with liquid argon as the active medium. This calorimeter subsystem consists of electromagnetic barrel and endcap systems, a forward calorimeter, and a hadronic end-cap calorimeter. It is designed to capture the energy of interacting objects, such as electrons, photons and jets in the electromagnetic calorimeters. This information is processed and propagated off the detector via the readout electronics system.

The readout electronics system can be broken down into the on-detector electronics and the off-detector electronics. The on-detector system samples cells at 40 MHz and sends the digitized pulse to the off-detector system for signal analysis and triggering. The off-detector system applies digital filtering to extract energy and time for each cell, and then passes the information to the trigger and data acquisition systems. For the HL-LHC, a full upgrade of the main readout chain is needed. The new readout will provide the full granularity of the LAr calorimeter to hardware triggering. This will be needed as the average number of interactions per bunch crossing will be increasing from 35 to up to 200 in the HL-LHC, and full information will be needed to maintain efficiency for physics analyses.

For the on-detector electronics, a new Front-End Board (FEB2) and Calibration Board are being developed. For the off-detector system, a LAr Timing System (LATS) and LAr Signal Processor (LASP) are being developed. In the following, each part of the on- and off-detector electronics will be described, together with their current status. The layout of the planned upgrade can be see in Figure 1, where the bottom half of the diagram illustrates the current system.

2. On-detector electronics

2.1 Calibration board

The Calibration Board is used to inject accurately calibrated signals directly onto the calorimeter cells. This provides a pulse of known amplitude and shape for the calibration and testing of the readout board channels. This board requires a 16-bit dynamic range, < 0.1 % linearity, and radiation hardness up to 14 kGy. 122 boards with 128 channels each are needed to calibrate the 182,468 calorimeter cells. The board uses custom ASICs, a "CLAROC" (HV CMOS 180nm technology (XFAB))that creates the pulse by opening a high frequency switch and a "LADOC" (CMOS 130 nm (TSMC)) that is used to select the calibration current. Version four of these ASICs are being produced, with an expected goal to overcome radiation and non-linearity issues. These are planned to be tested in late 2022. A 32-channel test board has passed specification review, and the next step will be the prototype development and testing.

2.2 Front-end board

There will be 1524 total FEB2 boards, each handling up to 128 channels. Each FEB2 will include a pre-amplifier shaper ASIC, an Analog to Digital Converter (ADC) ASIC, and lpGBT

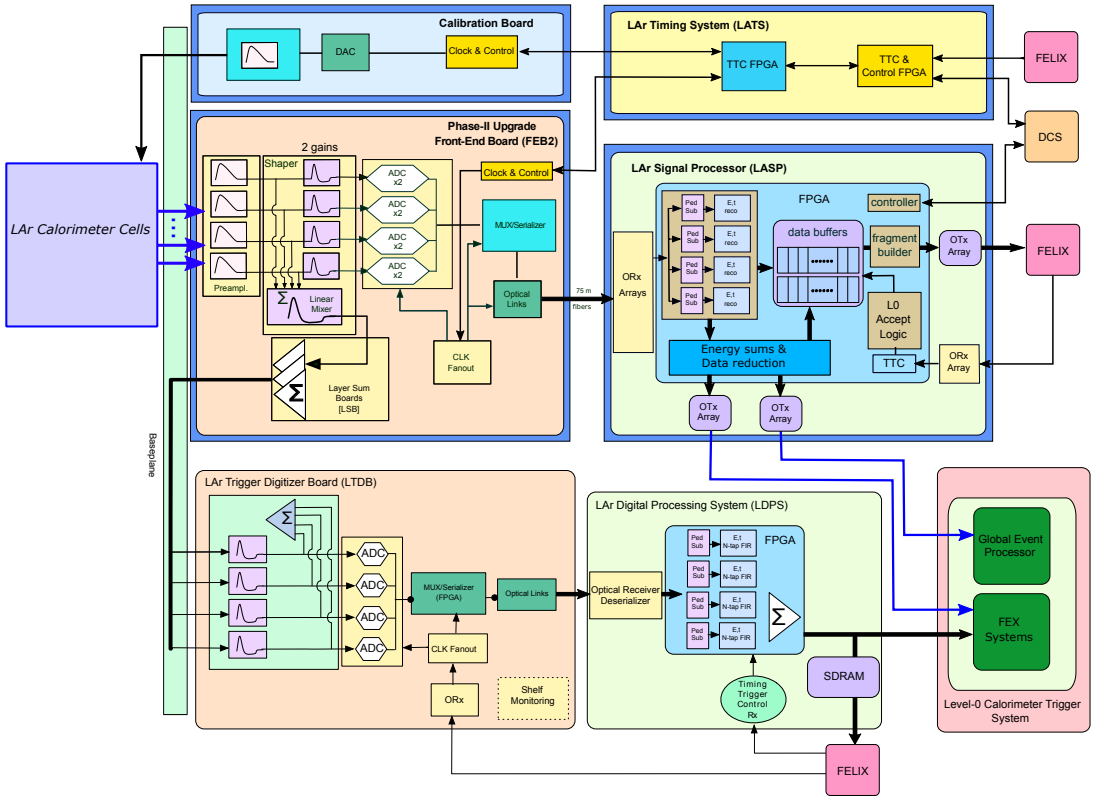

Figure 1: Phase-2 Architecture of the Liquid Argon calorimeter readout electronics.

chips connected to bidirectional VersatileLink+ transceiver modules. FEB2 test boards have been produced with 32 channels, validating multi-channel performance. Using this test board, control and readout on all channels has been tested. The next steps will be toward a 128 channel FEB2 prototype. A photograph of a FEB2 test board can be seen in Figure 2.

The pre-amplifier/shaper ASIC ("ALFE2") on the FEB2 provides analog processing of signals. It will amplify and shape ionization pulses in two overlapping gain scales, CR-RC^2 shaping, and will have 4-channel summing for the hardware trigger. It is required to have a large dynamic range (10 mA for 25 Ω channels, and 2 mA for 50 Ω channels), low noise and high linearity (< 350 nA for 10 mA channels and less than 0.2% deviation from linearity), and radiation tolerance (performant after a 12 kGy dose). The current ASIC version meets analog percision and radiation tolerance specifications.

The ADC ASIC ("COLUTA") has 8 channels and a 15-bit ADC. As of July 2022, 18 ADCs were tested over almost the full dynamic range and have achieved ENOB > 11 for a socketed chip and ENOB > 12 for a soldered chip. It has been integrated with the ALFE2 on a test board, which was planned for radiation testing in the fall of 2022.

Figure 2: Photograph of the FEB2 Slice Test Board. This is a full-size pre-prototype test board for the FEB2 featuring a quarter of the channels (32 instead of 128) and with pre-prototype versions of the ASICs (8 Pre-Amp and Shaper ASICs: LAUROCv2, 8 ADC ASICs: COLUTAv3, 8 lpGBTv0). The ASICs are placed in the same density as on the full 128 channel board.

3. Off-detector electronics

3.1 LAr timing system

The LAr Timing System (LATS) handles the trigger, timing and control (TTC) for 1524 FEBs and 122 Calibration Boards, with two links per board, based on an lpGBT protocol. It s an ATCA board ("LATOURNETT") which has one central and 12 "matrix" Cyclone10 GX FPGAs. There will be 26–30 boards in total. The schematic design is underway and a table test bench was recently developed. The central and matrix FPGA firmware was validated in simulation, the power-up sequence was verified with a POWERv2 board, and temperature tests have been run inside an ATCA crate. The next steps involve prototype submission and integration with the on-detector boards.

3.2 LAr signal processor

The LAr Signal Processor (LASP) and associated Smart Rear Transition Module (SRTM) are intended to apply digital filtering to the digitized waveforms from FEB2, calculate energy and time, and to transmit information to the trigger and data acquisition systems. Each LASP blade will receive information from 6 FEB2s, and will have two onboard Agilex FPGAs. The outputs of the system are to the global trigger system and the TDAQ. For the LASP, a first version of a test board exist with full capability to validate the power sequencing, I^2C sensors, clock, and FPGA configuration. Dedicated firmware has also been developed to receive and process data from a

FEB2 testboard. The next steps will be to take more measurements with the test board and full prototype design.

Another note is that machine learning is being investigated as a possible way to improve on the Optimal Filter approach [2] to energy reconstruction for the high pile-up conditions of the HL-LHC. Several kinds of neural networks and other algorithms are being explored as possible alternatives to be used in the data processing core of the LASP FPGAs.

4. Conclusion

The ATLAS Liquid Argon calorimeter on- and off-detector readout electronics will need to be replaced for the HL-LHC in 2029, in order to ensure the sucess of the physics program of the ATLAS Collaboration. These upgrades will address challenges associated with higher numbers of average interactions per bunch crossing, possibly increased center-of-mass energy, reading out the calorimeter at higher granularity, and a higher radiation environment. The development of these upgrades is continuing at a good pace. Many full custom LAr-specific ASICs are at or approaching the prototype stage, work is ongoing toward a full slice and systems test, and off-detector firmware continues to develop. The project is on-track for the HL-LHC.

References

[1] ATLAS Collaboration, ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report, ATLAS-TDR-027, https://cds.cern.ch/record/2285582.

[2] Stärz, Steffen, Development and implementation of optimal filtering in a Virtex FPGA for the upgrade of the ATLAS LAr calorimeter readout, 2012 JINST 7 C12017.