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# Prototyping Serial Powering with RD53A and ITkPixV1.1

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The high luminosity upgrade for the Large Hadron Collider at CERN requires a complete overhaul of the current inner detectors of ATLAS and CMS. These new detectors will consist of all-silicon tracking detectors. A serial powering scheme has been chosen in order to cope with the various constraints of the new detectors. In order to verify this new powering scheme and provide input for various system aspects, efforts are ongoing to set up a first larger prototype for serial powering using modules based on the new readout chips developed in 65 nm CMOS technology by the RD53 collaboration, RD53A and ITkPixV1. In particular, a serial powering stave consisting of up to 8 quad modules, either RD53A with planar sensor or ITkPixV1.1 without a sensor, has been set up in Bonn. This contribution covers the results obtained with RD53A modules and presents first measurements with a full ITkPixV1.1 serial powering chain, with emphasis on the electrical characterization of modules in a serial chain with representative services and power supplies.

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## 1. Introduction

In the context of the high luminosity upgrade of the LHC[2] the inner tracking detector of the ATLAS[3] experiment will be replaced by an all-silicon tracking detector, the ITk, consisting of 4 layers of silicon strips and 5 layers of hybrid pixel detectors. The future ITk pixel detector will feature approximately 8500 multi-chip modules with an active area of around 12.7 $m^2$, compared to 2000 modules and an active area of 1.7 $m^2$ in the current ATLAS pixel detector. As can be seen from Figure 1 the future ITk pixel detector will extend to significantly higher pseudorapidities up to $\eta = 4$. As parallel powering is not feasible, a serial powering scheme [4–6] has been chosen for the ITk pixel detector.

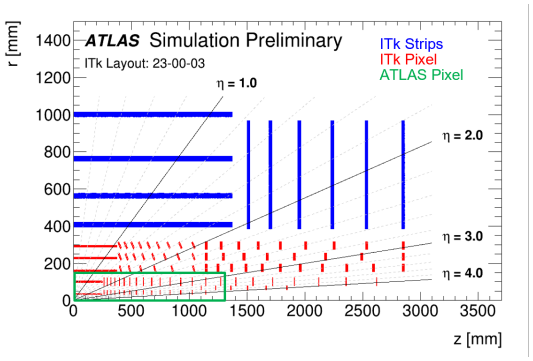



**Figure 1:** Schematic view of a single quadrant of the ITk detector, only active elements shown. Strip layers are shown in blue, pixel layers in red. The extent of the current ATLAS pixel detector is shown in green. Adapted from [1].

In this scheme a chain of pixel modules is supplied by a constant current. The supply voltage for each readout chip is generated by on-chip Shunt-LDO regulators, an LDO regulator with shunt capabilities. The input I-V characteristic of the Shunt-LDO resembles an ohmic resistor in series with a voltage source. The ohmic behaviour allows for current sharing between parallel Shunt-LDOs, while the series offset increases powering efficiency. Each readout chip will contain two parallel Shunt-LDOs to supply digital and analog domains of the chip. A typical pixel module in the ITk pixel detector will consist of 4 parallel readout chips with a total of 8 parallel Shunt-LDOs, which provides redundancy. The serial powering scheme has not been used in any large scale pixel detectors to date and provides new challenges for the electrical and mechanical design for the future ITk pixel detector. Consequently, serial powering requires extensive validation through system test efforts with representative prototype setups.

## 2. RD53A serial powering chain with planar quad chip modules

As one of several existing prototypes with different scopes, a dedicated serial powering prototype has been set up in Bonn with the intend of studying low level system aspects of serial powering, such as high voltage distribution schemes or Shunt-LDO supply current headroom. The prototype, which is shown in Figure 2, is loaded with up to 8 RD53A[7] quad chip modules with planar sensors, which are powered by a constant current source prototype. The setup uses dedicated, electrically representative services designs, which do not have to comply with constraints for the ITk pixel production services. Additional test points, which allow access to the on-chip voltage multiplexer as well as measurements of the on-module current distribution, are included on the module flex. These test points are accessible on the stave flex for each module, which also provides power and sensor bias voltage for the modules. On the stave flex each module can be bypassed as well as

separated from the high voltage supply. The End-of-Stave (EoS) card provides the interface to the readout system as well as power supplies. The serial powering chain return line, $LV_{Out}$, can be decoupled from the system reference potential on the EoS card, which allows daisy chaining of multiple serial chains to investigate longer serial powering chains. The high voltage distribution scheme can be freely configured using a set of jumpers and lemo connectors on the EoS card. The module uplinks and downlinks can be dynamically routed using two digital crosspoint switches on the EoS card, which are controlled using $I^2C$. Module readout and crosspoint switch configuration is performed using the BDAQ53[8] readout system. The full setup is designed with compatibility to ITkPix[9] modules on a dedicated module flex in mind.

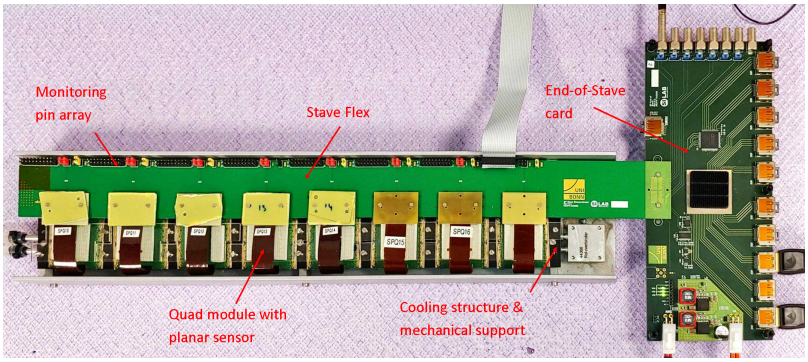



**Figure 2:** RD53A serial powering chain loaded with planar quad chip modules

## 3. Characterization of a serial powering chain with planar RD53A quad chip modules

The characterization program of the serial powering prototype covers several different aspects, ranging from measurements of the Shunt-LDO on module level to studies of system aspects of the full serial powering chain. Examples of this process are given in the following.

The electrical characteristic of each of the RD53A quad chip modules is dominated by the on-chip Shunt-LDO regulators and expected to behave like an ohmic resistor with resistance $R_{Eff} = R_3/k$ and series voltage $V_{Ofs}$, where $R_3$ is a known precision resistor on the module flex, $k$ a property of the Shunt-LDO and $V_{Ofs}$ being generated as a voltage drop over a dedicated resistor $R_{Ofs}$ on the module flex. The quad modules loaded on the structure are configured for a target working point $V_{In} = 1.6\,V$ at an input current $I_{In} = 4.5\,A$ with an offset voltage $V_{Ofs} = 0.9\,V$, including a supply current headroom of 20 % to account for uneven current sharing between regulators. An example measurement of the input I-V curve of a single quad-chip module is shown in Figure 3. A good agreement between measurement and the target values for $V_{Ofs}$ and $R_{Eff}$ is observed. Using the Shunt-LDO $k$ factor obtained from wafer probing data the current distribution between parallel Shunt-LDOs can be determined from the voltage drop over the slope resistor $R_3$. Figure Figure 4a shows the on-module current determined this way plotted against the supply current $I_{In}$. For most modules this yields an acceptable agreement considering the large uncertainties on $k$ from wafer probing, which are in the order of 10 %. In Figure 4b the current sharing on a single quad module, based on the calculated total module current from Figure 4a is shown. Based on the choice of slope

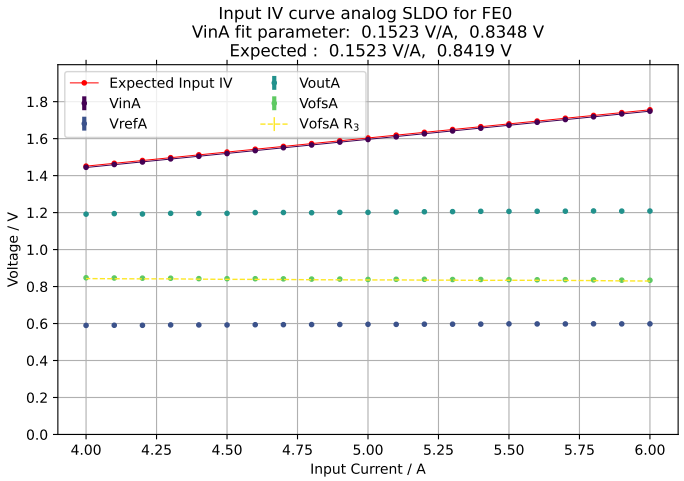
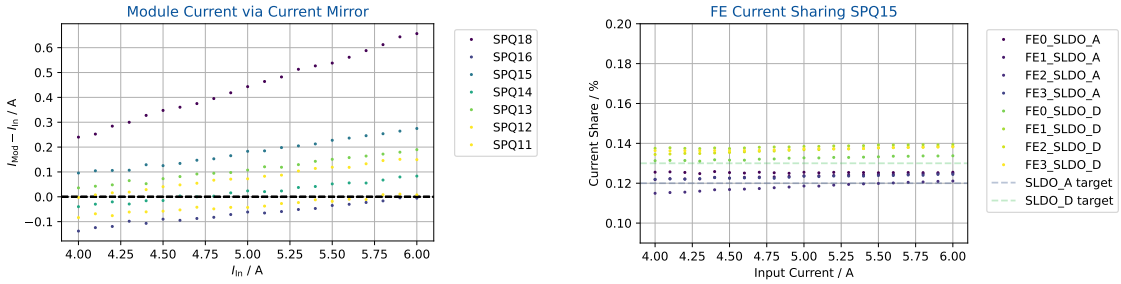



**Figure 3:** Example Shunt-LDO input I-V measurement of an RD53A quad chip module. Overlayed in red is the expected I-V behaviour based on the components loaded on the module flex and the $k$-factor determined from wafer probing data.



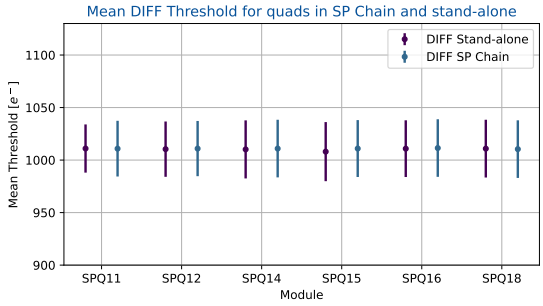

**(a)** Difference between determined on-module current and supplied module current plotted against the supply current $I_{\mathrm{In}}$ for modules in the serial powering chain. One of the quad modules has faulty Shunt-LDO and is excluded. The visible slope is caused by a dependency of $k$ on the supply current $I_{\mathrm{In}}$.

**(b)** Example current sharing between 8 Shunt-LDO on a single quad module plotted as a function of the supply current. By design, each digital Shunt-LDO is expected to draw 13 % of the supply current and each analog Shunt-LDO 11 %. Current sharing varies as a consequence of differing dependencies $k(I_{\mathrm{In}}$ for each Shunt-LDO.

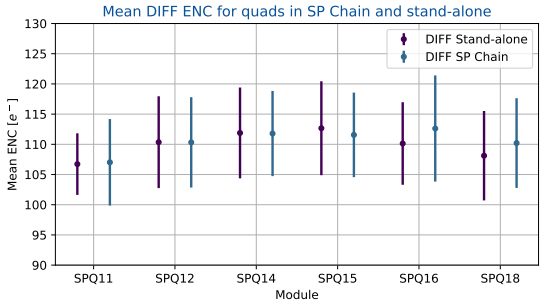
**Figure 4:** Calculated current sum on quad-chip modules and example on-module current sharing between Shunt-LDO. Uncertainties, which are dominated by the determination of $k$, omitted for better visibility.

resistors for the different Shunt-LDOs, a relative current share of 13 % per digital Shunt-LDO and 12 % per analog Shunt-LDO is expected. The measurements are in agreement with the expectation. Knowledge of the on-module current distribution between Shunt-LDOs is advantageous, as it allows optimization of the current headroom in the serial powering chain: the more uneven the current distribution between parallel Shunt-LDOs, the more headroom is required to supply each regulator with sufficient current. Future studies with ITkPixV1.1 quad chip modules are promising in this context, as the $k$-factor is known with much higher precision, which will allow for optimization of the Shunt-LDO working point and powering efficiency.

The performance of a serially powered detector is evaluated with respect to stand-alone module operation during reception tests. Key figures of merit are the threshold distribution after tuning

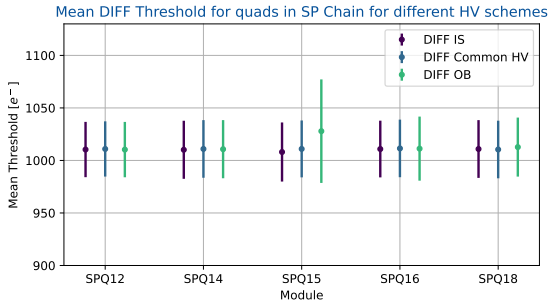



**(a)** Threshold mean of each module after tuning to a target detection threshold of 1000 $e^-$. Error bars denote the width of the threshold distribution.




**(b)** ENC mean of each module after tuning to a target detection threshold of 1000 $e^-$. Error bars denote the width of the ENC distribution.

**Figure 5:** Threshold performance and ENC for modules in serial powering operation compared to reception tests. Only measurements of the DIFF front end are shown.

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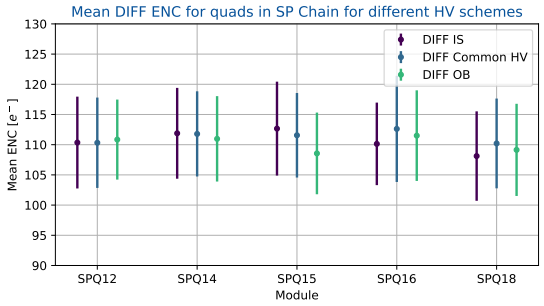


**(b)** ENC mean of each module after tuning to a target detection threshold of 1000 $e^-$. Error bars denote the width of the ENC distribution.

**Figure 6:** Threshold performance and ENC for modules in serial powering operation, comparing different high voltage distribution schemes. Only measurements of the DIFF front end are shown.

and the electrical noise. These performance figures are recorded during module reception tests and tracked during operation of the serial powering prototype. The initial module yield was acceptable with only two modules not being fully functional and masked in the following tests. The threshold performance is measured with respect to two of the three available analog front ends on RD53A, the linear (LIN) and differential (DIFF) front end, representing the choices of the analog front ends for the future CMS pixel detector and ITk pixel respectively. As shown in Figure 5 the threshold performance and ENC measurements in serial powering operation yield comparable performance to module reception tests. Similarly different high-voltage distribution schemes can be evaluated in terms of module performance. With the prototype setup available, three different high-voltage distribution schemes have been tested, the results being shown in Figure 6. These schemes correspond to the high-voltage distribution schemes forseen to be used in the inner system and outer barrel of the ITk pixel detector. In addition, a conventional setup with a common high-voltage supply line and return line for all modules in the serial chain was tested. Module performance in the different operating conditions is shown to be comparable with no detrimental impact observed based on the choice of the high-voltage supply scheme.

## 4. Summary and Outlook

In order to study low level serial powering system aspects, a small prototype setup has been integrated and characterised in Bonn. This setup consists of 8 RD53A quad chip modules with planar sensors in a serial powering chain with representative services. The accessible nature of the setup allowed a detailed characterisation of serially powered modules in varying condition. Module performance and electrical characteristics of the serial powering chain are shown to be good and meeting all expectations. At the time of writing, the prototype has been transitioned to ITkPixV1.1 quad modules without sensors and used to provide valuable measurements for the ITk pixel LV power supply market survey [10].

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