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Status of the LHCb Pixel Detector

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The LHCb experiment at CERN is a general-purpose forward spectrometer at LHC (CERN) optimized for heavy flavour physics and rare decays. It provides a coverage of $2 < \eta < 5$ with a momentum resolution of 0.5 % at pT < 20 GeV. A data-set of 10 fb⁻¹ has been collected at the end of Run 2, followed by a major detector upgrade (Upgrade I), fully replacing the vertex and trigger subsystems [1]. The Vertex Locator (VELO) is a silicon pixel tracking detector in the heart of the LHCb spectrometer. As a higher instantaneous luminosity of $2*10^{33}s^{-1}cm^{-2}$ is expected during Run 3 (2022 - 2025), the VELO has been upgraded by a brand-new detector. This new VELO replaces the silicon-strip technology with new 55 micrometers pitch pixels, operating as close as a 5 mm radius from the LHC beams. The VELO new readout ASIC, called VeloPix, is capable of operating at the 40 MHz collision rate, reaching 900 MHits/s. The detector is built with a modular design, composed of 52 modules divided into two-detector halves. The production of the required modules was completed in 2021, leading to the detector assembly phase. Both detector halves were successfully installed in May 2022. In this paper, the final steps of construction and installation will be shown. The detector is now under commissioning with beam and preliminary results will also be presented.

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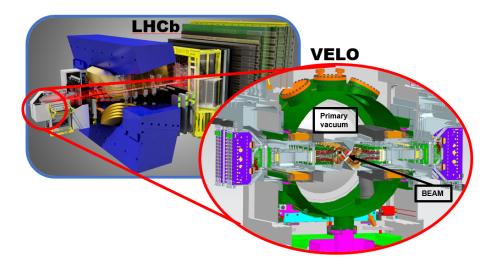


Figure 1: LHCb detector 3D view. Zoom and details of the VELO detector.

1. Introduction

LHCb is a forward spectrometer at LHC (CERN), aimed to study CP-violation in b-quark physics, but proven during the 2011-2018 data taking years to be a general purpose spectrometer with many exciting measurements. LHCb have been upgraded to further the physics performance during the Long Shutdown 2 (LS2). The luminosity have been increased by a factor five larger than Run 1 and 2. The hardware trigger have been removed and the detector will readout an event at every bunch crossing (40 MHz) using an efficient fully software trigger. This required new front-end electronics and new DAQ system.

2. Upgrade I Vertex Locator

The new Upgrade I Vertex Locator (VELO) is a hybrid pixel detector with planar silicon sensors, surrounding the interaction point of the LHCb experiment [2]. VELO is composed of two halves, which can be moved apart during beam injection and then returned to their nominal operating positions. Each half consists of a bank of 26 modules with a power dissipation 28 W each, separated from the LHC vacuum using a 150 um RF-Box. The closest distance of the active silicon to the LHC beam is 5.1 mm. This means that the silicon is at 900 μ m from the RF-box. The RF-box should be thermally stable and shield against RF pick-up the modules from the LHC beam. A 200 μ m n-on-p thinner silicon sensor was bump bonded to a custom made VeloPix ASIC. The sensors and the ASICs have to carried with a non uniform dose ($r^{-2.1}$) up to 400 Mrads for full lifetime. The readout chain of the VeloPix had to accomplish with the huge data bandwith, up to 20 Gbit/s for the central ASIC (Fig. 1). A Two phase evaporative CO₂ cooling is used to dissipate the detector power. This require that the 52 modules boil at the same time in the correct place. Moreover, a safety system has been built to avoid CO₂ leaks and prevent the damage of the RF-box, which could only support a δ P of 10 mbar between LHC and VELO vacuum.

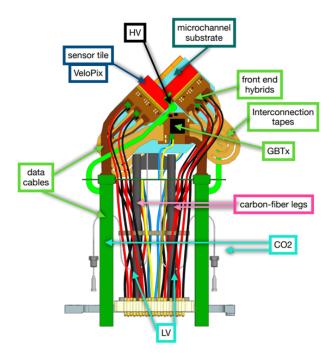


Figure 2: VELO module design.

3. Module Assembly

In Fig. 2, It is represented a schematic of the VELO module with the different parts. Each module is formed by a 200 μ m n-on-p silicon sensors bump bonded to a custom made VeloPix ASICs and the electronics to control and readout the chip. The module layout of the sensors is an L shape geometry with four sensor tiles, two on each side. Each tile consists of three VeloPix ASICs connected to a sensor. The VeloPix, based on the Timepix3, consists of a matrix with 256x256 pixels with a pixel size of $55x55~\mu\text{m}^2$. The VeloPix is thinned to 200 μ m to reduce the material budget and it is made in 130 nm CMOS technology. The readout architecture is data driven, zero suppressed, continuous, binary and trigger-less. The power consumption per chip is < 2W. The chip is optimized for electron collection, radiation tolerant up to 400 Mrad and protected from single event effects. The ASICs are mounted on a cooling substrate of 500 μ m silicon wafer with 120 x200 μ m2 microchannels [3]. A Two phase evaporative CO₂ cooling is used to dissipate up to 40W power at -30°C. The hybrid boards which provide the low and high voltage power and the control and readout communication are also mounted in the silicon substrate. After the module, all the rest of connectivity and electronics are placed: flex cables, vacuum feed-through board and opto-and-power board.

4. Commissioning

During the year 2022, the detector has been commissioned in the different aspects of its operation procedures. First of all, the safety system and the monitoring have been tested for a secure operation. Then, electrical test, communication test and cooling test have been performance.

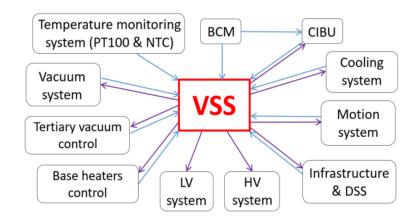


Figure 3: VELO Safety System interrelation with the different subsystems.

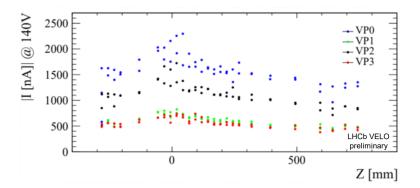


Figure 4: Leakage current vs Z position and sensor.

Finally, local and global commissioning with the rest of LHCb was carried on to calibrate the detector in terms of noise and equalization, time alignment or closing procedure.

4.1 Safety System

The VELO Safety System (VSS) is the responsible of the detector secure operation. It has bidirectional communication with the different subsystems (Fig. 3). The subsystems are not only part of VELO, some of them, like cooling plant or vacuum systems, are part of LHCb or LHC. More than 1200 temperatures are monitored for a proper control of the cooling and to turn off the Low and High voltage if it is needed.

4.2 Leakage current evolution

The radiation damage of the sensors need to be monitored for a proper performance of the detector. The high voltage will be increased during the run to fully depleted the sensors and to get a good charge collection efficiency. During the multiplicity scan was observed a linear current increase as it was expected. In Fig. 4 the leakage current of all the detector sensor is plotted after the full year of operation at a temperature of -30°C.

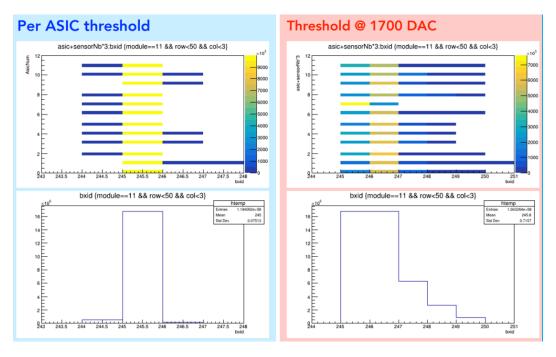


Figure 5: Time of arrival for an ASIC configured with the correct global threshold (left) or with a fix higher threshold (right).

4.3 DAQ and FPGA clustering

The DAQ controls the hybrid (SOL40) and acquires and processes the data (TELL40) using a FPGA [4,5]. The SOL40 system uses the LHCb standard protocol (GBT) to communicate with the GBTx ASIC while the TELL40 system uses the VELO specific protocol (GWT) to receive data from the VeloPix ASIC at 5 Gb/s for a total of 20 readout links per module. The TELL40 is in charge of collecting, decoding, reordering, processing and packing the incoming data before being sent to the computer network. The clustering algorithm has been integrated in the FPGA to reduce 11% the reconstruction sequence in the HLT1 [6]. Moreover, it reduce the power consumption by a factor 50.

4.4 Equalization and noise

The 65536 pixels of the VeloPix need to be equalized to react in the same way to the particles that arrive. There are two ways to equalize the VeloPix, one in terms of noise and another one in terms of gain. VELO equalization is based in noise scans. Each pixel has 16 possible threshold values for fine tuning. Moreover, the global analog parameters and threshold need to be set. It is needed to configure all the parameters for each ASIC. If not, different time of arrival per each pixel in the same ASIC could happen. In Fig. 5, the effect of calibrating or not the global threshold using analog parameters is shown. The bunch crossing ID (Bxid) of the LHC clock is used on the plot which represent the time of arrival.

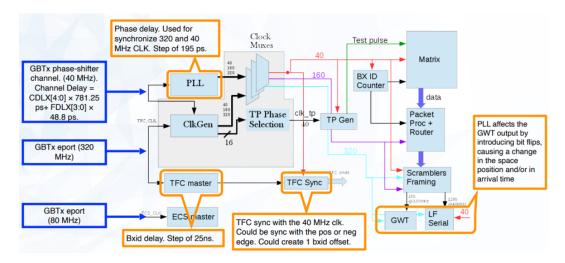


Figure 6: VELO module clock distribution.

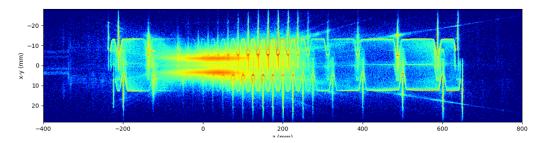


Figure 7: Z positions with vertex reconstruction.

4.5 Time Alignment

As mention in the previous section, it is needed to time align the VELO with the LHC clock and with the rest of the LHCb detector. In Fig. 6 the block diagram of the VeloPix clock distribution is represented with the input clock from the GBTx in blue and some explanation of the different parts in orange. The time alignment of the VELO depends on the FPGA control board that is place on surface, the GBTx and the VeloPix clocks and the Time fast control (TFC) synchronization with the LHC 40 MHz clock. Multiple scans have been done to understand the process for time align the detector. First, the stability of the transceiver was studied. It depends on the VeloPix PLL phase. Second, the coarse delay of the GBTx was scanned to find the clock phase regions that need to be avoid due to the TFC and LHC clocks synchronization in the VeloPix. Finally, the coarse delay of the GBTx was scanned with beam to find the proper time alignment phase.

4.6 VELO Closing and material scan

The VELO detector need to be open during injection of the LHC beams and close for physics data taking. Before the VELO halves can be safely closed, the positions of RF-boxes have to be verified. The verification is done by taking a map of reconstruct material interaction vertices, called material scan (Fig. 7). The detector have been successfully closed during the year 2022 with a ramp up on the number of colliding bunches to study the temperature and vacuum variation.

5. Conclusions

The new LHCb vertex locator was successfully constructed and installed in 2022. The detector was commissioned during the year with beam. First results on radiation damage and data rates were presented. Moreover, time alignment and ASIC equalization was performed. This allowed to reconstruct the first tracks, and therefore vertices. Material scans have been done for a safety close the detector to the data taken position.

References

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