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A High-Granularity Timing Detector for the ATLAS Phase-II upgrade

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The increase of the particle flux (pile-up) at the HL-LHC with instantaneous luminosities up to $L \simeq 7.5 \times 10^{34}\text{cm}^{-1}\text{s}^{-2}$ will have a severe impact on the ATLAS detector reconstruction and trigger performance. The end-cap and forward region where the liquid Argon calorimeter has coarser granularity and the inner tracker has poorer momentum resolution will be particularly affected. A High Granularity Timing Detector (HGTD) will be installed in front of the LAr end-cap calorimeters for pile-up mitigation and luminosity measurement. The HGTD is a novel detector introduced to assist the new all-silicon Inner Tracker (ITk) in the pseudo-rapidity range from 2.4 to 4.0, adding the capability to measure charged-particle trajectories in time as well as space. Two silicon-sensor double-sided layers will provide precision timing information for minimum-ionising particles with a resolution as good as 30 ps per track to help disentangle tracks from different vertices in the same bunch crossing. Readout cells have a size of 1.3 mm × 1.3 mm, leading to a highly granular detector with 3.7 million channels. Low Gain Avalanche Detectors (LGAD) technology has been chosen as it provides enough gain to reach the large signal over noise ratio needed. The requirements and overall specifications of the HGTD will be presented as well as the technical design and the project status. The on-going R&D effort carried out to study the sensors, the readout ASIC, and the other components, supported by laboratory and test beam results, will also be presented.

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*Speaker

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1. Introduction

The upcoming High Luminosity LHC (HL-LHC) upgrade will increase the instantaneous luminosity to $L \simeq 7.5 \times 10^{34} \mathrm{cm}^{-1}\mathrm{s}^{-2}$ [1]. Due to this increase, it is expected to have an average of 200 interactions per collision. To handle the increased pile-up, many parts of the ATLAS detector will be upgraded, among them the installation of a new all silicon inner tracker (ITk) [2]. In order to supplement the tracking performance in the forward region ($|\eta| > 2.4$), a new detector, the High Granularity Timing Detector (HGTD) [3], is planned to be installed in the endcap regions of ATLAS, as seen in Fig 1.

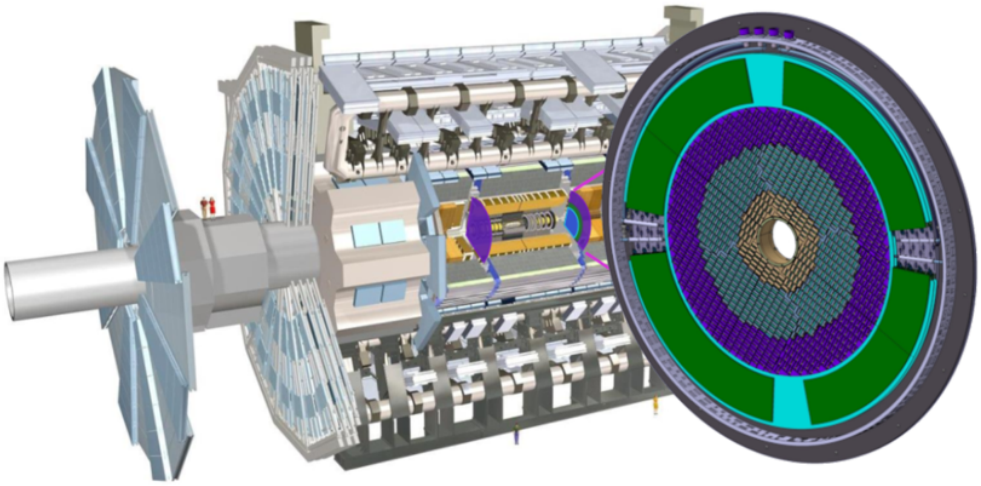


Figure 1: HGTD located on end-cap regions of ATLAS

HGTD will provide timing information to minimize the impact of the pile-up, as well as deliver bunch by bunch luminosity information. The detector is targeting a timing resolution of 30 ps per track at the beginning of the HL-LHC and 50 ps after a fluence of 2.5×10^{15} $\mathrm{n_{eq}/cm^2}$. It will cover the forward region with $2.4 \leq |\eta| < 4.0$. It is composed of 2 double sided layer disks mounted on a cooling plate. Each active layer on the disk has 3 rings with modules made of silicon sensors.

The active region of sensors contained in these rings will be covered with Low Gain Avalanche Detectors (LGADs). These silicon sensors will be bump-bonded to front-end ASICs that record the timing and hit information from the LGAD signal. Through wirebonds this ASIC connects to a flexible PCB, that relays this information to the peripheral electronics. From the peripheral electronics this information is sent to back-end servers through optical links.

These proceedings will briefly describe the R&D and current status of the LGAD and front-end ASIC in Sections 2 and 3 respectively. Section 4 is an overview of the development of HGTD modules, peripheral electronics and vessel followed by a description of the demonstrator project in Section 5.

2. LGAD sensor technology

LGADs are segmented planar n-on-p silicon sensors with an inner gain provided by a multiplication layer. This multiplication effect is produced by the highly doped p-layer under the n-junction.

Fig 2 shows a cross-sectional drawing of an LGAD sensor with the multiplication layer in blue. When a charged particle passes through the sensor, it creates an electron-hole pair. The hole is absorbed by the substrate, while the electron moves in the direction of the multiplication layer. As this electron goes through the multiplication layer it creates more electron hole pairs, which repeat the same process of the original pair, thereby creating a large discharge current through the sensor. This avalanche current can then be detected by front-end electronics. Due to their internal gain and thinness LGADs can provide fast timing measurements. Additionally, depending on how doped the thin gain layer is, the sensors can also be radiation hard.

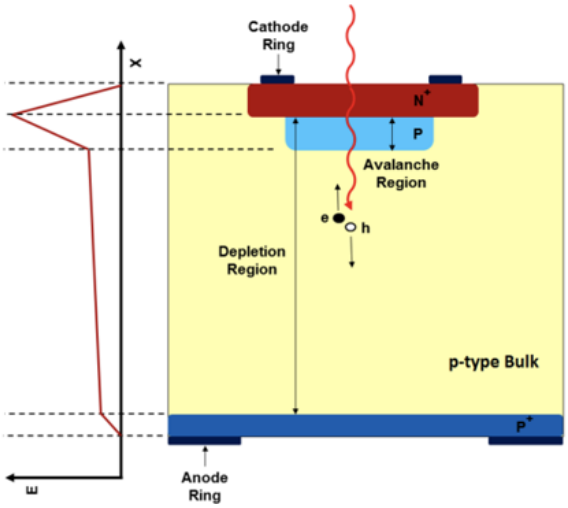


Figure 2: Cross-sectional drawing of LGAD [3]

An LGAD pad size of 1.3 mm × 1.3 mm and thickness of 50 µm was set as a baseline due to the occupancy requirements. Smaller pads yield better spacial resolution but also increase the amount of relative inactive area due to the inter-pad gap that has no gain. A HGTD full size sensor will be composed of 15 × 15 pads. HGTD is collaborating with multiple producers for this R&D phase, as well as for the production phase. Sensors from various providers such as CNM, FBK, HPK, IHEP-IME and USTC-IME were produced and tested.

2.1 Single Event Burnout (SEB)

In previous testbeams in 2021 a maximum operational voltage was identified due to the SEB. When operating at high bias voltages, the sensors would suffer a powerful discharge that rendered them unusable. Fig 3 shows a crater that results from such a discharge. A possible cause for this event is a breakdown of the electrical field at high bias voltages. This breakdown is related to the bias voltage, as well as the thickness of the sensors. Through many test-beam tests a "safe zone" of 11 V/µm was identified, as illustrated in the Fig 4.

Sensors with carbon infused gain layers were identified as a possible solution, as they are more radiation hard and do not require as high an increase in the bias voltage with increased levels of fluence. Multiple sensors with carbon infused gain layers were produced at various providers. These were then irradiated and tested at the test-beam sites in DESY, Germany, and SPS, CERN.

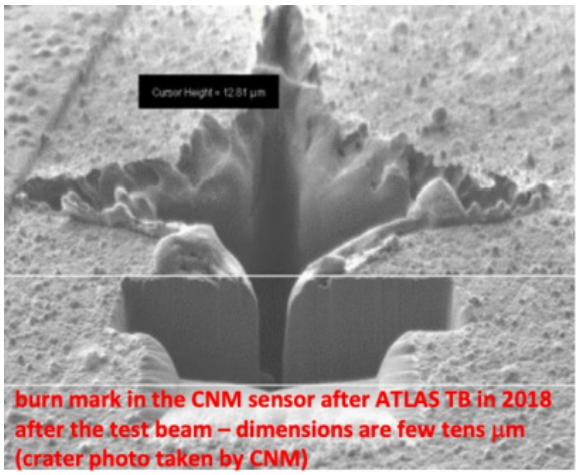


Figure 3: Crater created by SEB

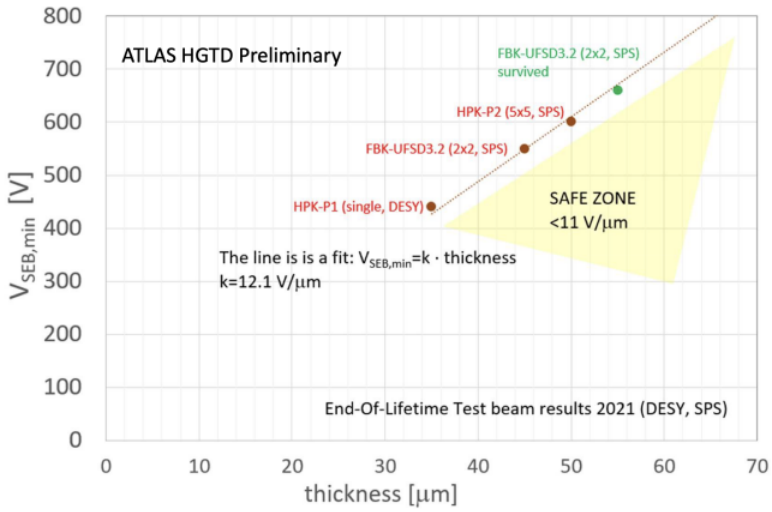
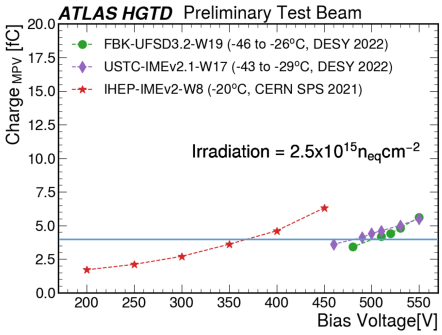


Figure 4: Sensors end-of-lifetime tests. Results show a correlation between thickness and maximum bias voltage and indicate a "safe zone" of 11 V/µm

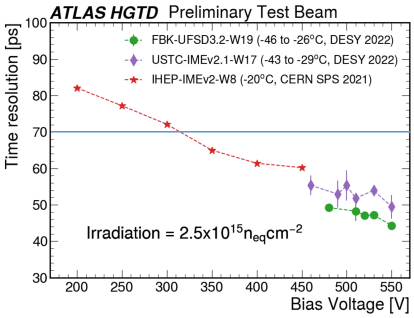
All carbon infused gain layer sensors met the HGTD requirements up to the highest fluence level of 2.5×10^{15} n_{eq}/cm^2. As shown in the plots in Fig 5a and Fig 5b these sensors reach a 4 fC collected charge and a 70 ps timing resolution at the highest required fluence level below the SEB range. The plot in Fig 5c also shows high efficiency at 1.5×10^{15} n_{eq}/cm^2.

3. HGTD ALTIROC ASIC

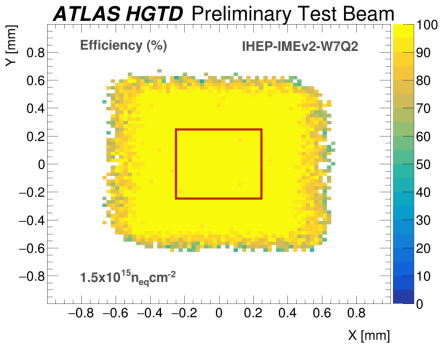
The ALTIROC is the front-end HGTD ASIC that interfaces with the HGTD LGADs. It has 225 channels that are bump bonded to a full size sensor. These channels contain an analog front-end that features a pre-amplifier and discriminator to detect the LGAD signals. The discriminator output



(a) Charge collection at highest fluence



(b) Timing resolution at highest fluence



(c) Efficiency of IHEP-IMEv2-W7Q2 sensor at 1.5×10^{15} n_{eq}/cm^2. Global efficiency of the sensor is calculated from the ROI in the central area of the detector (inside the red $0.5 \times 0.5 mm^2$ square).

Figure 5: Plots of charge collection, timing resolution and efficiency of irradiated carbon infused gain layer sensors

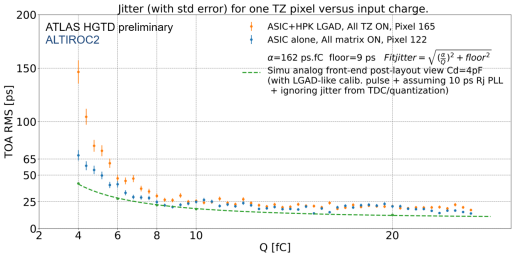
leads to 2 Vernier Timing-to-Digital converters that register the Time of Arrival (TOA) and Time Over Threshold (TOT) of the signal. This timing data is stored on local digital registers.

The timing requirements for this ASIC are quite strict. It needs to reach a jitter of 25 ps at 10 fC input charge and a jitter of 70 ps at 4 fC charge. These charge levels represent the expected charge collection of the sensors at the beginning and at the end of the life-cycle. The ASIC also needs to trigger the discriminator at a threshold of 2 fC, while maintaining a high efficiency.

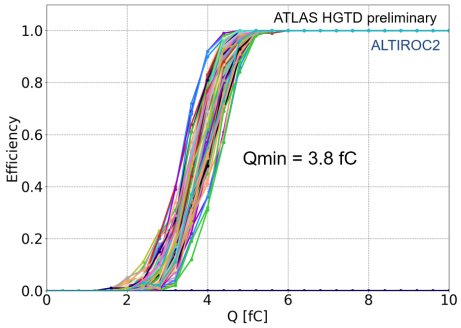
In 2022 the ALTIROC 2 version of the ASIC was produced, which features most of the final requirements. It has all 225 channels, voltage and transimpedance pre-amplifiers, local digital memory and a data serializer for communication. The discriminator threshold, TOA, TOT, jitter and other important requirements were verified.

This version of the ALTIROC was also used to produce hybrids, which is an ASIC bump bonded to full-size sensors. Multiple hybrids were successfully assembled. As the plot in Fig 6a shows the TOA jitter of the hybrid is higher than that of the bare chip and does not meet HGTD requirements. The plot in Fig 6b also shows that only a minimum threshold of 3.8 fC was obtained. After many tests parasitic capacitances between the sensors and the pre-amplifier were identified as the most likely cause. Tests with updated boards that have different input capacitor values are

ongoing, and have shown an improved behaviour.



(a) Jitter comparison of a single channel between simulation, a bare ALIROC and a ALTIROC plus sensor hybrid at various levels of injected charge



(b) Efficiency of all transimpedance channels on a hybrid sensor at various levels of injected charge

Figure 6: Plots of jitter and efficiency for ASIC plus sensor hybrid

4. Modules, detector units and vessel

HGTD modules are composed of two hybrids attached to a module flexible PCB. HGTD will produce in total 8032 modules in 6 separate institutes around the world. The dimensions of the modules are 2 cm × 4 cm. The module flex is glued to the upper inactive side of 2 sensors. Then it is wirebonded to the sensor and ASIC, for the HV biasing and ASIC readout and powering respectively.

The modules need to be attached to detector units so as to be mounted on the HGTD cooling plate. HGTD will have 13 unique detector unit designs per side (as shown in Fig 7) that will have differing configurations and hold a different amount of modules. This number of detector units was chosen to optimize the assembly procedure and minimize gaps between readout rows.

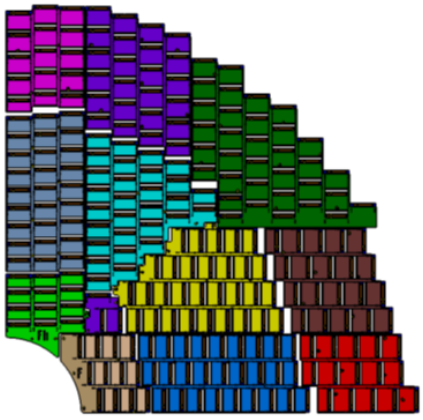


Figure 7: Detector units configuration in a quadrant

The modules on the detector units communicate with the peripheral electronics through long flexible PCBs called flex tails. These flex tails carry the power, HV bias, data and controls signals.

There will be tails of varying lengths depending on the radius of the module. On the longest readout row there will be a stack of 19 flexes, as a result the thickness requirements are quite strict. Prototypes of these flex tails have been assembled and are under test. The physical qualities of the connection itself are being tested, as well as the signal quality when there is also HV and power going through the flex tail.

The peripheral electronics boards are located just outside the active region of the HGTD disk in $640\,\text{mm} < r < 920\,\text{mm}$. There will be 6 unique board designs per quadrant. The design of these boards is complex due to high density of components located on the board. The densest board connects to 55 modules, and a schematic of this board has been made and now a layout and routing of the board with all components is ongoing. To test individual components of these PCBs, modular PCB boards have been assembled as shown in Fig 8. These contain DC-DC converters, a Versatile Link+ Transceiver (VTRX+) and 2 low-power gigabit transceivers (LpGBTs), for timing and luminosity data. These boards allow for tests of a basic readout chain by connecting to a server on one side and ASIC emulators on the other.

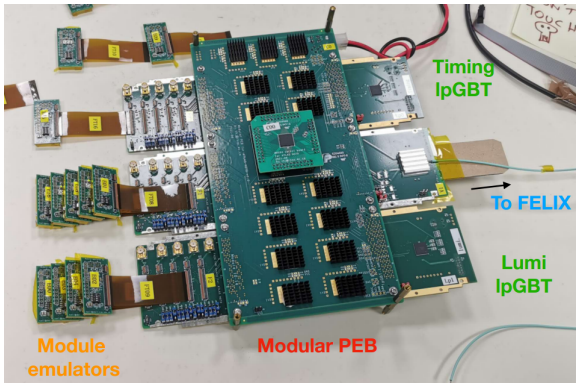


Figure 8: Modular PCB board

HGTD double-sided disks will have three rings with modules surrounded by peripheral electronic boards on both sides of a cooling plate. Two of these doublesided disks and an internal moderator are located inside the HGTD vessel in-between a front and back cover with an outer ring around for feedthroughs, as shown in Fig 9. The modules need to be operated at $-30\,^{\circ}\text{C}$. Therefore the active layers are mounted on an aluminum cooling plate that has titanium cooling pipes inside. Each half-disk cooling plate will have 8 serpentines that are cooled through liquid CO_2. The inside of the vessel and the cooling plate will be grounded so that it functions as a Faraday cage, protecting the modules from electromagnetic noise. There is ongoing work on the design of the feedthroughs for CO_2, and feedthroughs for all electronic and optical signals on the outer ring.

5. Demonstrator

The demonstrator project has the goal of verifying various parts of the overall HGTD project. One of the first parts the project was the heater demonstrator, which was built to verify the CO_2 cooling capabilities and identify the best thermal media between modules and the cooling plate. For there to be an effective thermal conductivity to the CO_2 liquid in the pipes, there can be no air

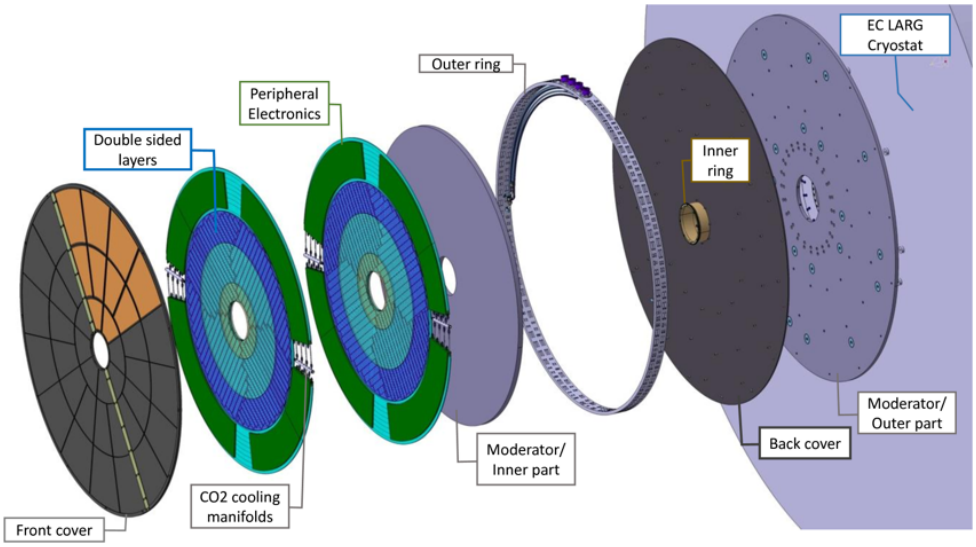


Figure 9: HGTD vessel drawing

pockets in-between the bottom of the modules and the cooling plate surface. As it is not possible to guarantee a completely flat surface and uniformity in the detector units, it is necessary to have a more malleable media in the middle. Small module sized silicon heaters were manufactured and mounted on a prototype one row support. These rows were then loaded on a stave with cooling pipes inside, as seen in Fig 10. These heaters have built-in RTDs which were used to verify the quality of the thermal media below. Tests show that two graphite sheets with a bit o thermal grease in-between demonstrated the best thermal performance.

Figure 10: silicon heaters mounted on stave

Another element of the heater demonstrator are tests on the innermost serpentine with a smaller scale cooling plate. This cooling plate was fitted with Kapton heaters that are powered to give an equivalent amount of heat dissipation to the estimated one of the modules on the inner serpentine.

Another part of the demonstrator project is the DAQ demonstrator. This demonstrator is intended to build a complete DAQ chain using the modular board referenced in Section 4. With this board a successful communication link was established between module emulators and a backend server. The LpBGTs on the board were configured and received valid messages through the VTRX+ optical interface. Tests are ongoing with digital modules (ASICs with a module flex) through a

small flex tail.

The final goal of the demonstrator project is the full demonstrator. This will feature 55 modules mounted on detector units connected to a prototype peripheral electronic board. This structure will be mounted on a cooling plate and connected to a backend server. The goal is to read all 55 modules successfully and maintain them at a stable and safe temperature. This will be the main goal of the HGTD demonstrator project in 2023.

6. Conclusion

HGTD is a new detector for ATLAS that will provide timing information to minimize pile-up noise in the forward region. The goal is a 30 ps track timing resolution that can go up to a 50 ps track timing resolution at the highest estimated fluence. A dedicated R&D campaign was done and established that LGAD sensors with carbon infused gain layers can meet the requirements up to the highest fluence. ALTIROC 2 was manufactured, which is the most recent version of the HGTD front-end ASIC. The bare ASIC fulfills the requirements and tests on the ASIC attached to sensors are ongoing. On the demonstrator project, tests to verify the planned cooling system are ongoing, as well as the DAQ readout chain, with the endgoal of developing a full demonstrator that integrates these elements simultaneously with real modules and electronics.

References

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