

MoTiC: Prototype of a Monolithic Particle Tracking Detector with Timing

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MoTiC (Monolithic Timing Chip) is a prototype DMAPS Chip that builds on sensor technology developed in the ARCADIA project. The 50 by 50 μm^2 pixels contain a small charge collecting electrode with a very low capacitance surrounded by radiation-hard in-pixel electronics. The chip contains a matrix of 5120 pixels on an area of 3.2 by 4 mm^2 . Each pixel features a trimmable and maskable comparator with a sample and hold circuit for the analog pulse height. Groups of 4 pixels share a TDC situated also in the readout matrix. This work presents the chip design and preliminary results of the hit efficiencies and spatial resolution measured in a first test beam campaign with 4-5 GeV/c electrons conducted at DESY.

*10th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Pixel2022)
12-16 December 2022
Santa Fe, New Mexico, USA*

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1. Introduction

The high energy physics group at Paul Scherrer Institut (PSI) in collaboration with ETH Zürich has started an R&D program for generic development of depleted monolithic active pixel sensors (DMAPS). The aim is to develop prototypes with moderate radiation hardness and timing resolution for potential use in low energy particle physics experiments at PSI. Several production process technologies are being evaluated. This paper describes a first prototype implemented in the LFoundry 110 nm CMOS process.

2. Production Process

MoTiC is manufactured in a modified 110 nm CMOS process by LFoundry. These modifications and the development of the sensing structure have been carried out by the ARCADIA collaboration [1–3]. A cross section of a fully processed device is sketched in Fig. 1. The chip is processed on a high resistive substrate onto which an epitaxial layer is grown. A deep p-well is used to house and shield the in-pixel circuits. Small area n^+ -implants form the low capacitance charge collection electrodes.

A large area p^+ -implant is added on the backside to form a junction that depletes the sensor. It is surrounded by a set of guard rings that step down the high voltage towards the chip edge. This involves non-standard back side photolithography and mask alignment between the two sides of the wafer. The depletion starts at the backside and grows towards the pixels. Full depletion is therefore needed in operation to electrically isolate the collecting electrodes from each other. The results presented here were obtained with 200 μm thick samples, that were operated with a bias voltage of -100 V and a leakage current of 30 μA . The devices were proven to be operational with backside voltages between -65 V to well below -100 V.

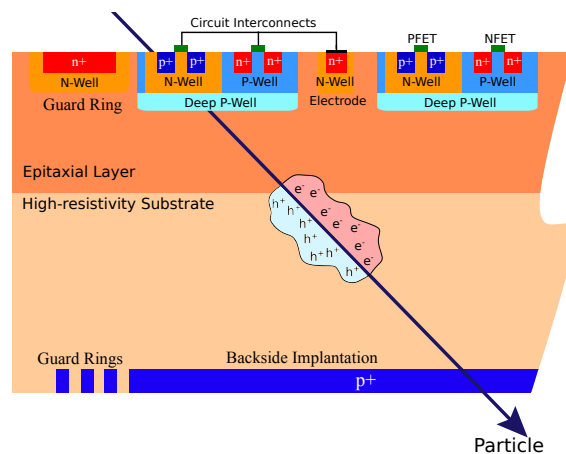


Figure 1: Cross section of the modified 110 nm LFoundry process.

3. Architecture

MoTiC features 5120 pixels arranged in 80 columns and 64 rows with a 50 by 50 μm^2 pitch. There are a total of 7 different preamplifier designs in different sections of the matrix. Three different preamplifier topologies and 5 variations in the feedback circuitry of one of the topologies are implemented. The high-level view of the in-pixel schematics is shown in Fig. 2. At the input node to the preamplifier a configurable calibration charge can be injected. The output of the preamplifier is written onto the sample and hold capacitor. If the signal crosses the threshold of the trimmable comparator, the sample and hold switch is opened after an adjustable delay and the pulse height is stored on the capacitor. The switch can also be opened for all pixels simultaneously with an external hold signal. The output of the comparator is latched in the hit flip flop for subsequent readout.

Pixels are selectable with two shift registers and are read out sequentially. When the read signal is applied to a selected pixel, the pulse height and state of the hit flip flop are transmitted on a column bus to the column periphery before they are sent off chip for digitization. The current architecture does not feature a zero-suppressed readout, so the full matrix needs to be read out.

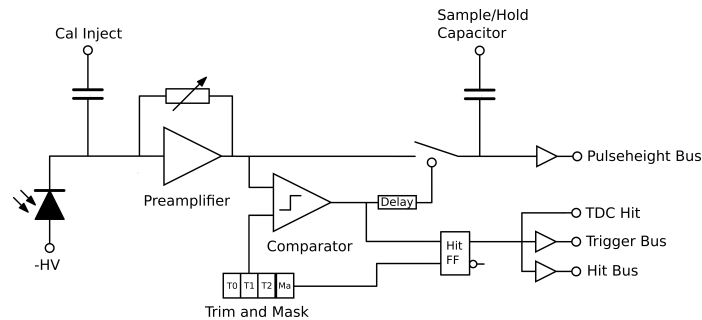


Figure 2: Schematics of the pixel unit cell of MoTiC.

4. Test Beam Setup and Readout Mode

The results presented in these proceedings have been obtained in Nov. 2022 at beam line 24 at the DESY test beam facility [4]. A telescope consisting of 6 ALPIDE layers [5] is used to track the 4-5 GeV/c electrons with a spatial resolution of less than 5 μm . The coincidence of two scintillators mounted on the downstream side of the last layer is used for triggering. The device under test (DUT) is mounted between the third and fourth layer of the telescope. The beam is limited to a size of 5 by 5 mm^2 by a collimator thus leading to a track yield (i.e. tracks in the DUT) of about 50 % when reading out the full matrix of 12.8 mm^2 .

The readout sequence is started with a delay of approximately 200 ns after the scintillator trigger. This delay is composed of signal propagation times, the TLU processing and the processing of the trigger signal on the DAQ board. Firstly, the external hold signal is applied to store the pulse heights in all pixels on their respective sample and hold capacitor. Then a full frame of pulse heights is read out sequentially. The in-pixel discriminator and TDC are not enabled for the measurements presented here. An offline per-pixel threshold of 10 times the RMS of the pedestal distribution is

applied to discriminate hits. The majority of the pixels has a pedestal RMS of less than 5 ADC counts, while typical signal levels are at least several 100 ADC counts.

5. Hit Efficiency and Spatial Resolution

The analysis in the following section was performed with the Corryvreckan framework [6]. The telescope is aligned using χ^2 minimization of tracks that are reconstructed with a general broken line model [7].

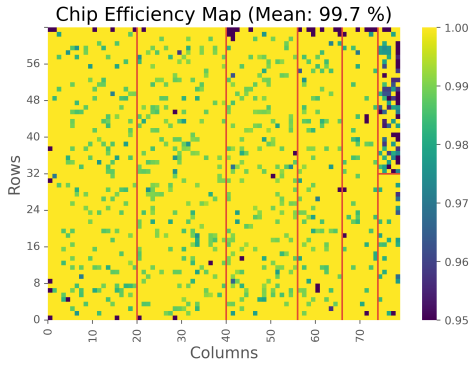


Figure 3: Hit efficiency over the full matrix. The red lines indicate the boundaries between the different preamplifier designs.

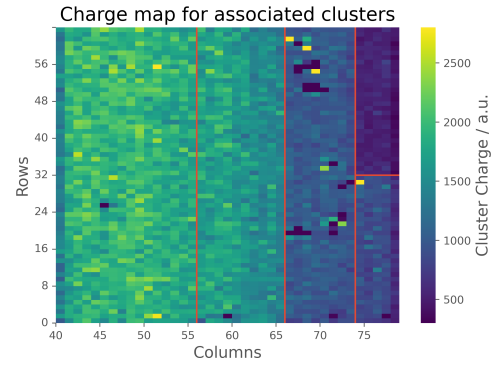


Figure 4: Map of associated cluster charges of right half of the chip.

All measurements are obtained at vertical incidence with unirradiated samples at room temperature. The hit detection efficiency of the chip was determined with approximately 400 thousand tracks. The efficiency is defined as the ratio of associated clusters in the DUT to the number of reconstructed tracks traversing the DUT. The per-pixel hit efficiencies are shown in Fig. 3. The boundaries between pixel flavours with different preamplifier designs are drawn in red. All regions are almost fully efficient, except in the top right flavour. This flavour features a larger feedback capacitance in the preamplifier that lowers the gain considerably leading to a lower efficiency. The overall hit efficiency over the full matrix is over 99.7%.

A map of pedestal-subtracted charge for clusters associated to a track in the right half of the chip is shown in Fig. 4. The charge is shown in arbitrary units, as no calibration of ADC counts to electrons is available yet. The difference in the amount of collected charge is clearly visible between the different preamplifier designs, with the top right falling significantly short of the other designs.

The track residuals are defined as the difference between the intercept of the track with the DUT and the center of gravity of the associated hit cluster in the DUT. A distribution of track residuals after the DUT alignment is depicted in Fig. 5. The standard deviation of the residuals is taken as the hit resolution of the DUT. The shown residual distribution, that is convoluted with the telescope resolution, has a standard deviation of 10.0 μm . This is significantly less than the resolution in absence of charge sharing of a 50.0 μm pitch pixel, which is $\frac{50.0 \mu\text{m}}{\sqrt{12}} \approx 14.4 \mu\text{m}$. This can be explained with the significant charge sharing taking place even at vertical incidence.

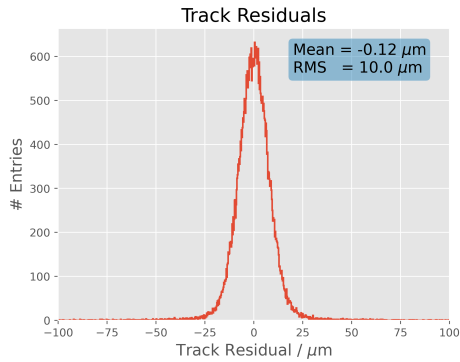


Figure 5: Distribution of track residuals after DUT alignment.

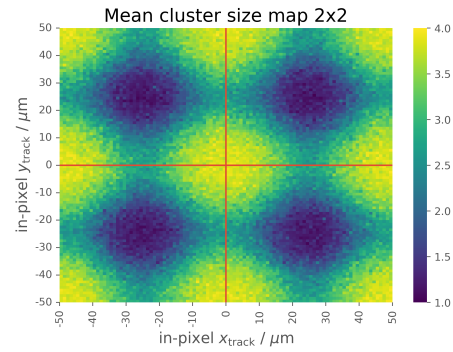


Figure 6: 2 by 2 map of position dependent mean cluster size.

Evidence for this charge sharing is shown in Fig. 6. Hits in a small region in the center of the pixel lead to a cluster size of 1, but larger clusters are formed when the hits take place closer to the pixel borders.

Conclusions

In this work we presented first measurements with a novel fully depleted monolithic active pixel chip. A hit efficiency in excess of 99.7 % and a spatial resolution of 10.0 μm at vertical incidence were demonstrated. While the TDC functionality has been verified on test structures in the lab, the in-pixel TDC remains to be tested. Furthermore the operation in test beam with the comparator rather than an external trigger and an offline threshold will be carried out in future test beam campaigns.

Acknowledgements

The authors would like to express their gratitude to the ARCADIA collaboration for their offering to participate in their engineering runs and for their input during the design phase. The development of the process modification and sensor nodes has been performed in the framework of the INFN CSN5 Call ARCADIA. The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). Finally, the authors thank the developers of Corryvreckan for their efforts to develop a framework that significantly facilitates the analysis of the test beam data. Individuals have received support from the European Unions Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant105 agreement No 884104 (PSI-FELLOW-III-3i) and the Swiss National Science Foundation.

References

- [1] L. Pancheri et al., *A 110 nm CMOS process for fully-depleted pixel sensors*, *Journal of Instrumentation* **14** (2019) C06016.
- [2] L. Pancheri et al., *Fully Depleted MAPS in 110-nm CMOS Process With 100-300 um Active Substrate*, *IEEE Transactions on Electron Devices* **67** (2020) 2393.
- [3] C. Neubüser et al., *Sensor Design Optimization of Innovative Low-Power, Large Area FD-MAPS for HEP and Applied Science*, *Frontiers in Physics* **9** (2021) .
- [4] R. Diener et al., *The DESY II test beam facility*, *NIMA* **922** (2019) 265.
- [5] M. Mager, *ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade*, *NIMA* **824** (2016) 434.
- [6] D. Dannheim et al., *Corryvreckan: a modular 4d track reconstruction and analysis software for test beam data*, *Journal of Instrumentation* **16** (2021) P03008.
- [7] Claus Kleinwort, *General broken lines as advanced track fitting method*, *NIMA* **673** (2012) 107.