PROCEEDINGS OF SCIENCE

Monolithic Stitched Sensor (MOSS) Development for the ALICE ITS3 Upgrade

G.H. Hong[a,b,*] **on behalf of the ALICE collaboration**

[a] *Yonsei University,*
50, Yonsei-ro, Seoul, South Korea
[b] *CERN,*
1211, Geneva 23, Switzerland

E-mail: ghhong@yonsei.ac.kr

The Monolithic Stitched Sensor (MOSS) chip is the first stitched prototype developed for the upgrade of the Inner Tracking System 3 (ITS3) vertexing detector in the ALICE experiment at the LHC. This upgrade aims at reducing the material budget to 0.05% X_0 per layer, achievable with a large bendable single-die sensor by replacing the water-cooling system with air flow and minimizing other external circuit components. Thus the only material remaining in the acceptance is the silicon itself. Benefiting from the stitching technology, the MOSS chip measures 1.4 cm × 26 cm and is designed to explore the feasibility and yield factors of wafer-scale sensors. The chip is implemented in a 65 nm CMOS imaging technology, studied in the framework of the CERN-EP R&D. Composed of one left endcap, 10 repeated sensor units, and one right endcap, it features more than 20 sub-units to increase power granularity and hence resilience to manufacturing faults. Such design presents a number of challenges. This contribution gives an overview and then focuses on the multiple-domain power plan and its impact on domain isolation and electrostatic discharge protection.

10th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Pixel2022)
12-16 December 2022
Santa Fe, New Mexico, USA

*Speaker

PoS(Pixel2022)028

1. Introduction

During the Long Shutdown 2 (LS2) of the CERN Large Hadron Collider (LHC), the Inner Tracking System (ITS) of the ALICE detector was upgraded with increased vertexing and tracking performance. This new ITS (ITS2) adopted the ALPIDE (ALice PIxel DEtector) chip, which is a CMOS Monolithic Active Pixel Sensor (MAPS) enabling the integration of sensor and readout electronics in a chip [1, 2]. Approximately 24,000 ALPIDE chips are arranged on 7 cylindrical layers surrounding the beam pipe and covering a 10 m^2 area with about 12.5 billion pixels.

The ALICE collaboration is developing a wafer-scale bendable monolithic CMOS particle sensor to replace the inner barrel of the ITS during the LHC LS3 [3, 4]. The primary benefit of this upgrade is to reduce the material budget significantly so that the new vertex detector improves the tracking precision and efficiency. The main concept of this detector is the following. First, a wafer-scale sensor chip that measures up to 270 mm $\times$ 94 mm will be produced from a 12-inch wafer. Then, the wafer is thinned down to about 50 µm before dicing to make it bendable. A bent silicon die alone allows a stable and self-supporting mechanical structure. No circuit board is required for electrical connections in the sensor acceptance region. Power density is kept below 20 mW/cm^2 for cooling with air instead of water. In the end, the ITS3 only needs 6 functional wafers, not counting spares. However, there is already interest in the ITS3 chip for other experiments, and such a chip is an important milestone for future developments.

This contribution presents some of the design challenges of the MOnolithic Stitched Sensor (MOSS) which is a development prototype chip towards the ITS3 detector [5]. First, the stitching technology, which enables such a large sensor in the standard CMOS process, is introduced in Section 2. The chip architecture and main features of the MOSS are presented in Section 3. Section 4 addresses its design challenges in terms of the power and the pad ring. Section 5 concludes the paper with a summary and an outlook.

2. Wafer-scale sensor

In the CMOS fabrication process, photolithography is the process of transferring a pattern from a masking reticle onto a silicon wafer. This pattern-transferring step is repeated, moving to the next area making the same patterns to cover the whole wafer area. Since each pattern transferred onto the wafer is independent of each other, a chip larger than the reticle size cannot be produced in conventional photolithography. Due to the limitation of the size of the exposure field of the lithography stepper, the reticle size is only a few centimeters in each dimension.

The stitching technique makes the patterns at the lithography boundary continuous by abutting and aligning each lithography step to the previous one. This allows continuous metal traces to cross the boundary of the different stitches to realize chips larger than a single exposure. Stitching can be done in 1-dimensional or 2-dimensional direction, as shown in Fig. 1. In both cases, the green part is the repeated inner section and the rest is for enclosing the inner section. The final detector for the ITS3 will be implemented with 2-D stitching.

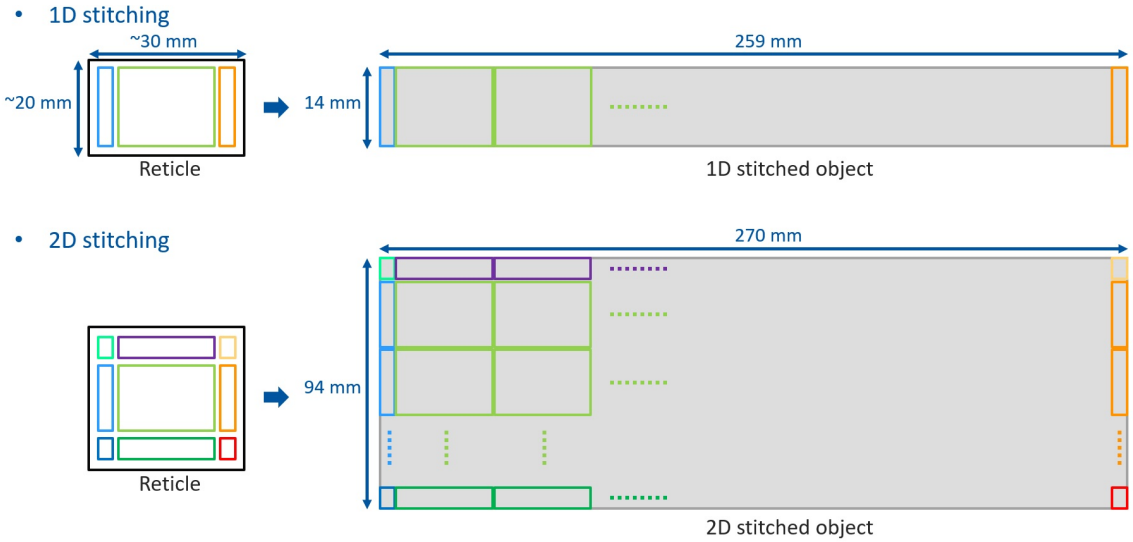

Figure 1: Stitching technique.

3. Chip architecture

The MOSS chip is a prototype towards the stitched sensor for ITS3. The MOSS is not yet at full wafer scale for the final chip.

The technology selected for the MOSS is TPSCo 65 nm Image Sensor CMOS process using 300 mm wafers. This technology provides the stitching technique which allows full wafer-scale sensor design.

Figure 2 (a) shows the design reticle where the layout of the three MOSS blocks, H, B, and E, are placed along with several small test chips. H, B, and E sections for the MOSS are the left endcap, the right endcap, and the repeated sensor unit (RSU), respectively. The transfer of E section onto a wafer is repeated 10 times abutting each other, and H and B sections enclose the repeated units at each end using the stitching technique, as shown in Fig. 2 (b). The overall chip dimensions are 259 mm x 14 mm and 6 MOSS chips are manufactured per wafer.

The primary goals of the MOSS chip are to learn the stitching technique to make a particle detector, to learn about the yield, to learn how to make interconnects for power and signals on a wafer-scale chip, and to study IR drops, leakage currents, spread, noise, and speed experimentally.

The RSU is subdivided into an upper half and a lower half, with 4 pixel matrices each, as shown in Fig. 3. The top matrices feature a pixel pitch of 22.5 µm whereas the bottom ones 18.0 µm. Since the pixel has almost the same circuit component, the layout density of the bottom and top is different; the bottom has a compact layout while the top maximizes the width and spacing of structures for yield. Based on the front-end nominal current of 30 nA, the analog power density is 7 mW/cm^2 for the top matrix, and 11 mW/cm^2 for the bottom. There are a total of 80 matrices in 10 repeated units with 6.75 million pixels and 736.3 million transistors over an area of 14 $\times$ 259 mm^2. A negative bias can be applied to the substrate for high charge-collection efficiency.

Figure 4 shows the conceptual diagram of the MOSS chip and the simplified logical organization of the signaling in the matrix. The matrix features binary readout with parameterizable strobe

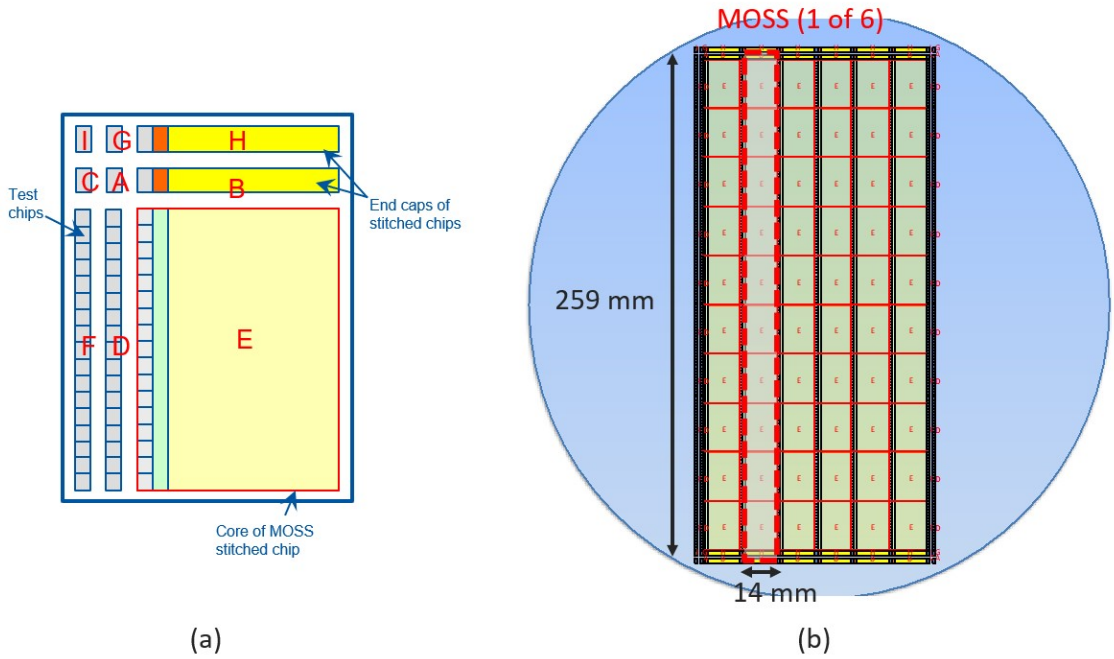

Figure 2: (a) Design reticle and (b) its wafer product.

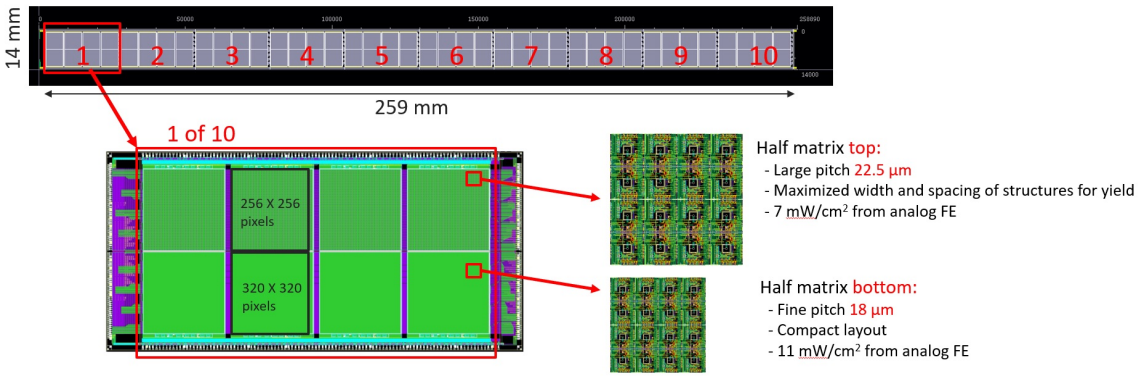

Figure 3: The MOSS chip showing main features of top and bottom halves.

duration. The pixel has an in-pixel latch with fast OR gate for row and column output signals. The readout of the hit information is zero-suppressed; it sequentially encodes the address of pixels with a hit as in ALPIDE [6]. Each analog front-end can be tested with analog charge injection and each pixel digital logic with a digital pulse. Noisy pixels can be masked by setting the MASK_ROW and MASK_COLUMN signals.

4. Design challenges

The chip architecture should be tolerant to manufacturing faults in order to secure the yield of such a large wafer-scale chip and to quantitatively analyze the yield. The chip has a segmented powering scheme to avoid that a single fatal fault kills the entire chip. By having power granularity,

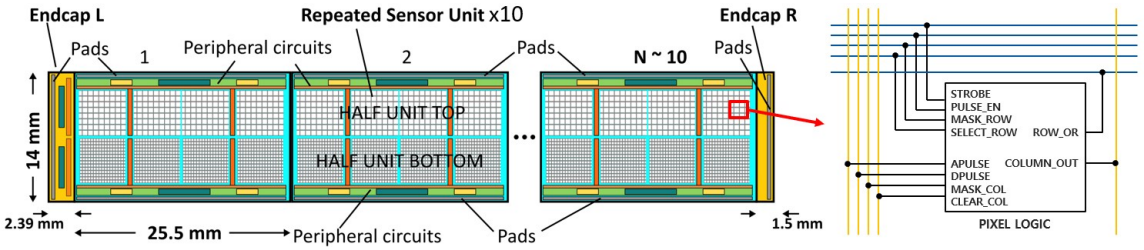

Figure 4: Concept diagram of the MOSS chip and its pixel configuration.

sub-units of the chip can be tested independently even though other parts of the chip have shorts preventing powering.

Several layout techniques are also adopted to improve the yield. The matrices are designed with Design for Manufacturing (DFM) rules; all widths and spacing are increased and multiple contacts and vias are placed instead of single ones wherever possible. The digital periphery circuits are implemented with a standard cell library customized to respect the DFM rules.

4.1 Power plan

The final design is segmented in 20 sectors since each RSU is divided into top and bottom. Each sector can be powered and operated independently. Any sectors that have fatal short can be turned off while others are still operative. Each sector has analog and digital core domains and an IO domain. There are two additional domains for each inter-domain communication circuit at top and bottom and one global net for the substrate bias. In total, 65 power domains exist in one chip. Any domains of the 20 half-units can be powered from the long edge and/or from the power pad on the short edge, as shown in Fig. 5.

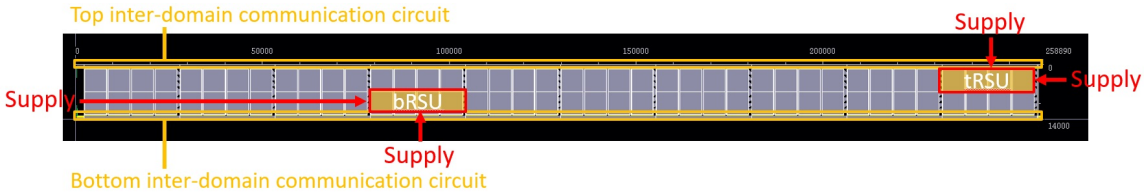

Figure 5: An example of powering the half-units.

Each half-unit can be controlled and read out through the long edge or the left endcap short edge, thanks to inter-domain communication circuits located at the top and bottom. Figure 6 shows an example of the MOSS testing scenarios. The top RSU2 and the top RSU4 are controlled and read out through the top inter-domain communication circuit and the left endcap. The top RSU9 is electrically disconnected from the top inter-domain communication circuit and controlled through dedicated pads on the long edge. All the other domains are off. In this way, the twenty half-units will be tested independently, studying the yield of the half-units and its possible dependence on the layout density. In addition, the yield will be quantified at various levels of granularity: at matrix level, at column or row level, or at the single pixel level.

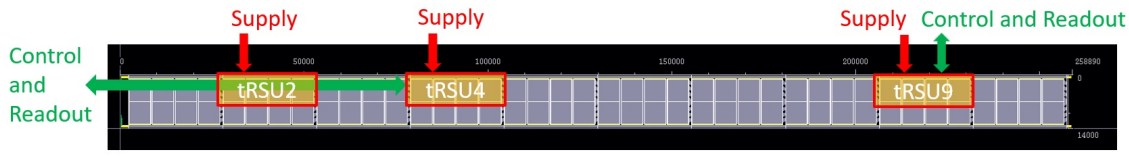

Figure 6: An example of the testing scenarios.

4.2 Domain isolation

The proposed power scheme requires the isolation of the wells of the different power domains. The area of the reverse-biased junction also needs to be reduced as much as possible for the yield. Since the standard well structure does not provide deep N-well isolation, as shown in Fig. 7 (a) where the deep N-well is continuous across the entire region, several domain isolation cells are customized. Figure 7 (b) shows how the domains are isolated with the customized separation cells in the pad ring region. The deep N-well is separated by a deep N-well cut cell and a substrate bias cell is placed in between domains. Isolation extension cells are also introduced to reduce the area of the reverse-biased junction in the domains. This results in the deep N-well being cut over the full width of the isolation structure.

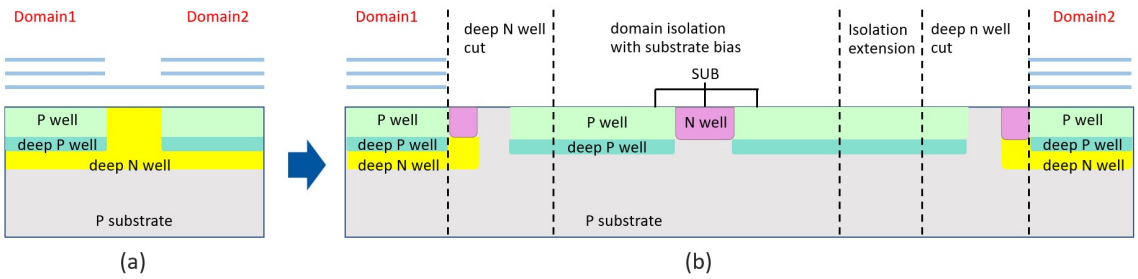

Figure 7: Domain isolation implementation.

4.3 Electrostatic discharge protection

The standard electrostatic discharge (ESD) protection structure is not compatible with the power scheme of the MOSS chip given the possibility of the negative bias at the substrate. The inter-domain communication block must be able to operate while the other domains are off, and vice versa. Considering that power and ground of the off-domains should be held at the same voltage as the substrate, the inter-domain ESD protection circuit should be robust to voltage differences from 0 V up to -1.2 V in both directions.

Since the inter-domain signaling occurs between the inter-domain communication block and the digital domains of each half-unit, 4-diodes strings are introduced as an inter-domain ESD structure between the communication block and the digital domains in both directions, as shown in Fig. 8. Power clamp diodes are also added to the inputs of the inter-domain signaling buffers to protect input gates.

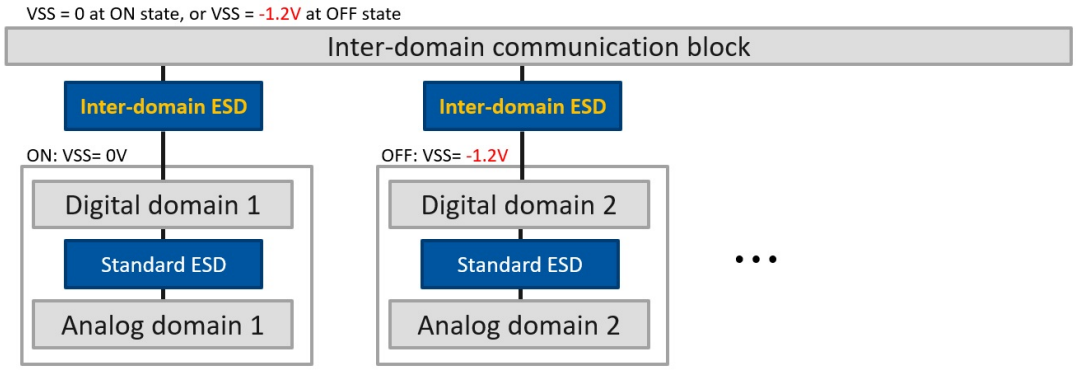

Figure 8: ESD protection scheme.

5. Conclusions

The MOSS chip is developed as a proof-of-concept of a stitched monolithic particle detector for the ITS3. The architecture and the design challenges are described. Power granularity is introduced to cope with manufacturing defects. The DFM rules are followed for the yield. Domain isolation is implemented to be compatible with the powering scheme. The inter-domain ESD protection circuit is customized due to negative bias at the substrate.

The final artifacts file for manufacturing was sent for production in November 2022. The final artifacts file was sent for production in November 2022. The chip is expected to be ready for testing in June 2023 and extensive testing will follow. The lessons from the design phase and the testing will be incorporated into the next prototype development towards the first-ever wafer-scale monolithic sensor applied to high-energy physics.

References

[1] M. Mager *et al.*, "ALPIDE, the monolithic active pixel sensor for the ALICE ITS upgrade," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 824, pp. 434–438, 2016.

[2] G. A. Rinella *et al.*, "The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 845, pp. 583–587, 2017.

[3] L. Musa and W. Riegler, "Letter of Intent for an ALICE ITS Upgrade in LS3," CERN-LHCC-2019-018, https://cds.cern.ch/record/2703140?ln=en, Tech. Rep., 2019.

[4] A. Kluge *et al.*, "ALICE-ITS3—A bent, wafer-scale CMOS detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 1041, p. 167315, 2022.

[5] P. V. Leitao *et al.*, "Development of a stitched monolithic pixel sensor prototype towards the ITS3 upgrade of the ALICE Inner Tracking System." TWEPP, 2022.

[6] P. Yang *et al.*, "Low-power priority address-encoder and reset-decoder data-driven readout for monolithic active pixel sensors for tracker system," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 785, pp. 61–69, 2015.