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Alternative Approach to Front-end Amplifiers Design for Timing Measurements with Silicon Pixel Detectors

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The increase in luminosity and pileup foreseen for future colliders has recently pushed central pixel detector technology towards an increase in timing resolution. Increased time resolution can ease track reconstruction by adding a more precise timestamp to events for better track separation. An alternative approach to timing with silicon pixel detectors is proposed in this paper. Current approaches are based either on amplitude increase due to avalanche charge multiplication or in the reduction of charge collection time in a 3D geometry detector. Both approaches uses charge integration amplifiers for signal pre-amplification. The main feature of the proposed approach is based on current preamplifier signal readout and a more comprehensive approach to time resolution improvement. An additional aspect of this approach is that it shifts the attention from the detector design to the readout electronics design. The current pulse of a silicon detector has an intrinsically fast (in the order of 5 ps) rise-time however the actual rise-time of a detector connected to a current (low impedance) preamplifier is limited by the RC product of the input resistance and the capacitance of the detector/preamplifier interface and the bandwidth of the preamplifier itself; using low impedance amplifier and low capacitance pixel detector the rise-time of this pulse can be kept below 200 ps. The amplitude of the signal can be increased by bias overvoltage and temperature reduction (increases mobility shrinking the current pulse duration). Furthermore low temperature operation (- 30 °C or less) and the low input capacitance of the detector can help to reduce noise. The combination of reduced rise-time, increased amplitude and reduced noise can tentatively improve the overall time resolution below 20 ps which is considered the best result achieved.

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1. Introduction

The forthcoming hadron collider experiments, starting from HL-LHC, will have to face the problem of keeping an excellent performance concerning efficiency, resolution, and background rejection for all final state particles and physical quantities used in the analysis of the data despite the very high luminosity of the colliding beams. The challenge posed by the very high rate of concurrent collisions per beam crossing ("pileup") at these collider experiments requires vertex detectors with the ability to discriminate tracks and vertexes not only by using their space resolution but also by acquiring timing informations [1]. Under the HL-LHC beam condition, with luminosity, in excess of 10^{35} $cm^{-2}s^{-1}$, the pileup will be in the order of 150-200 and 10-20% of vertexes identified by the inner tracking detector will be actually composed by the overlap of two subsequent pp collisions that happened so close to each other to be mistakenly interpreted as a single interaction. Fig. 1 shows an event display of a bunch crossing in future collider.

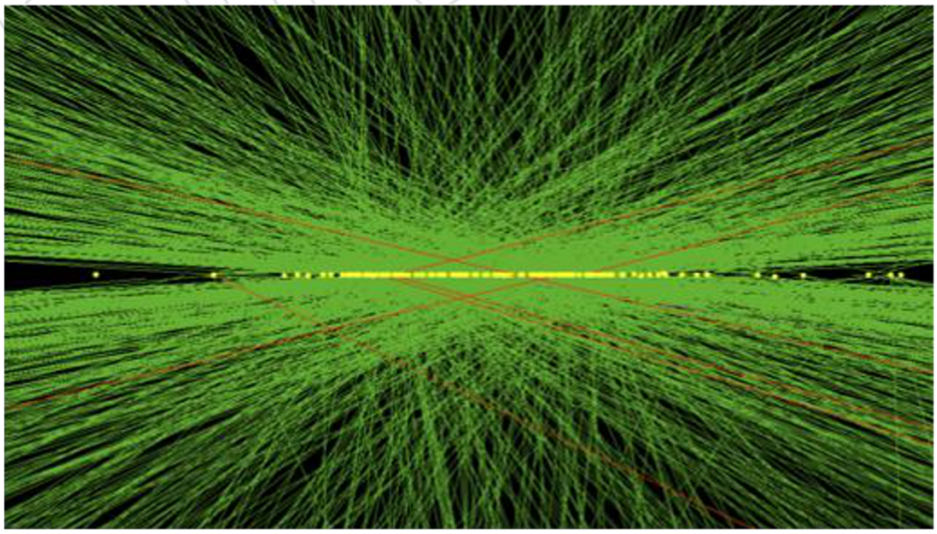

Fig.1 Distribution of vertex (Yellow dots) on a 200 pile-up bunch crossing event. The RMS of the spread in vertex position is 5 cm.

In order to disentangle the overlapping vertexes it is necessary to associate to each track a time-stamp: since the time spread of the interaction happening at each bunch crossing (25 ns) is of the order of 100-150 ps, a time accuracy of about 30-40 ps or better will allow to associate the correct track to two spatially overlapping vertexes.

For these purposes an effort has been devoted to the development of position detectors having precise time resolution (≈ 20-30 ps) and two different approaches have been considered up to now: the LGAD approach and the TIMESPOT approach. In order to compare the two previous approaches and the alternative approach proposed here, we should consider the following equation [2]:

$$\sigma_t = \frac{\sigma_N}{dV/dt} + \Delta t_{lan} \approx t_r\left(\frac{\sigma_N}{A_V}\right) + \Delta t_{lan} \qquad (1)$$

This equation gives the time resolution σ_t at the time pickoff (e.g. the discriminator threshold), σ_N is the voltage noise, dV/dt is the slew rate of the signal, Δt_{lan} is the contribution of the time walk due to Landau fluctuations, t_r is the rise-time and A_V is the signal amplitude.

The LGAD approach [3,4,5] proposes a low-gain avalanche silicon detector, namely a silicon pixel detector with a gain of 10 generated by an internal avalanche charge multiplication mechanism. A simple scheme of the detector is shown on Fig.2. Low-Gain Avalanche Diodes, as developed by CNM [6], are n-in-p silicon sensors with a high ohmic p bulk which have a p++ implant extending several microns underneath the n-implant The extra deep p++ layer creates a strong electric field that generates charge multiplication.

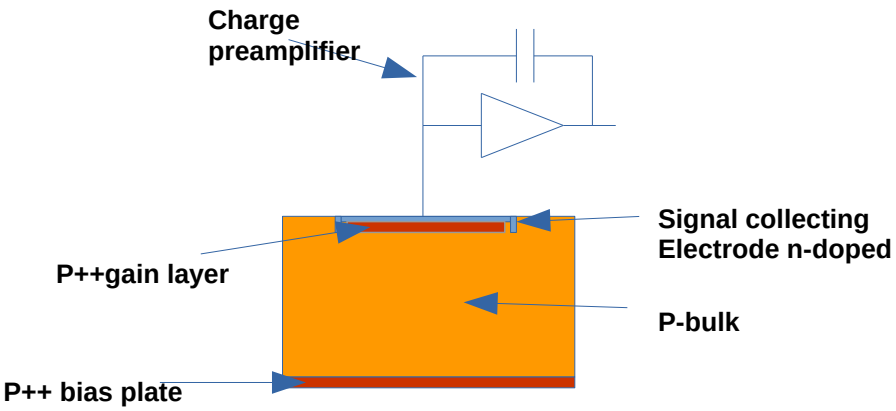

Fig.2 Low Gain Avalanche device basic scheme

Referring to equation 1 the strategy adopted in this approach for the reduction of time resolution (σ_t) is the increase, by charge multiplication, of the factor A_V (compared to a simple pixel device) and also a reduction of charge collection time (related with the reduced thickness of the detector) that imply a reduction in t_r. The shape of the current pulse from the detector that is integrated by the input stage of the front end electronics that is a charge integrator is shown in ref. [4], the rise-time of the integrated pulse in the order of 1 ns.

In the perspective of using these devices in HL-LHC experiments those detectors have been radiation tested and their performances have been evaluated before and after various levels of irradiation, Time resolution of various detector types has been measured and reported in ref [7] at different irradiation levels namely: 0 n_{eq}/cm^2 , 0.8 x 10^{15} n_{eq}/cm^2 , 1.5 x 10^{15} n_{eq}/cm^2 , 2.5 x 10^{15} n_{eq}/cm^2 . As reported time resolution changes from about 25 to 45 ps in unirradiated devices to about 40 to 60 ps in irradiated devices with the highest fluence. Temperature dependence of timing resolution has also been studied [5] in order to evaluate how temperature affects time resolution due to noise reduction (σ_N in equation 1) . From the various detector channels we have a resolution spread from 49 to 64 ps at 20 °C that becomes from 32 to 43 ps at -20°C.

The TIMESPOT approach is based on silicon 3D detectors with trench-shaped electrodes, the structure of a single detector cell is shown in Fig.3 seen from the top. The trench-shaped form of the electrodes is preferred to the more usual (in 3D detectors) finger-shaped form because it generates a homogeneous field that improves the position-dependent collection time spread. The strategy adopted in this approach is the reduction of the charge collection time

because of the reduced collection distance of the electrodes (25 µm); a reduction in charge collection time in a charge integrating front-end preamplifier implies a reduction of rise-time that, according to equation 1, improves the time resolution.

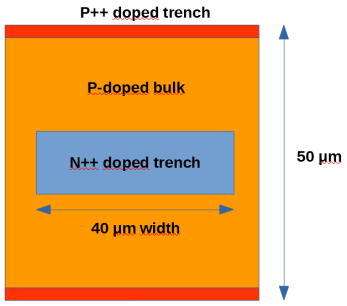

Fig.3 TIMESPOT detector layout (one cell) seen from top.

Time resolution measurements using this approach have been performed in a beam test at PSI [8]. The data acquisition was performed using a 8 GHz bandwidth, 4 channel oscilloscope and the analysis was performed on digitized data. Using the analysis method call reference method (described in ref. [8]) and a bias voltage of -140 V, it was possible to achieve a time resolution of $\sigma_t = 20.6 \pm 0.4$ ps. Furthermore the TIMESPOT collaboration has developed a laser-based characterization system in order to study the detector and electronics performances and optimize their design, it is also important to precisely measure sensors time response over their active area. This goal can be achieved using a custom laser-based setup to deposit a known energy in specific regions of the pixel sensitive volume, allowing us to estimate the performances of these sensors under charged-particle incidence.

2. An alternative approach to front-end preamplifier design

The present approach towards the improvement of time resolution is based on three pillars

1. **Current pulse electronic readout**
2. **Low temperature operation**
3. **High bias voltage below the multiplication regime**

The two approaches previously described are based on the charge integration of pulses but this is a limit because the rise-time of the pulse (see equation (1)) corresponds to the collection time of the charges inside the detector. The TIMESPOT approach tries to go beyond this limit by reducing the charge collection space (and therefore the charge collection time) but this cannot be reduced above a certain limit otherwise the channel density becomes too high. The minimum collection time (= risetime in equation (1)) achieved by TIMESPOT is in the order of 300-400 ps. In order to overcome this limit the alternative approach, here

described, uses an electronic current pulse readout instead of the integrated charge pulse readout. The shape of a current pulse inside a typical detector is shown in Fig.4.

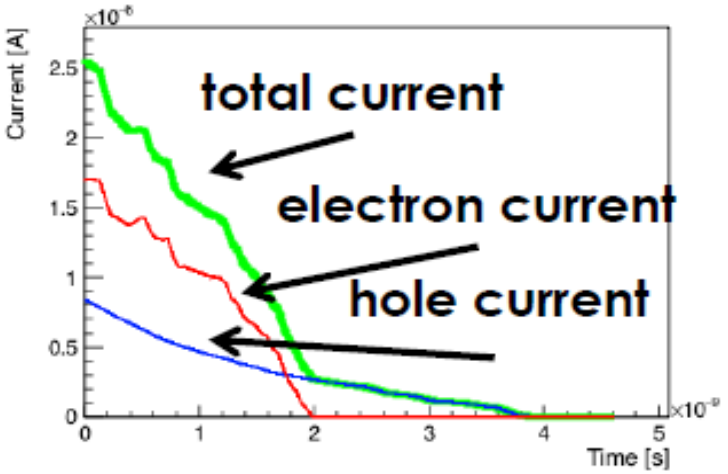

Fig.4 Current pulse in a typical planar silicon detector: Due to the different mobilities of the holes and of the electrons, the electron contribution last less (around 2 ns instead of 4 ns) and has higher current amplitude compared to the hole current. The usual approach of integrating current pulses leads (in this case) to a charge pulse having about 3 ns risetime while using current pulses the rise-time may reach ideally the value of 5 ps (not shown in the graph because too short).

The rise-time of this current pulse is ideally in the order of 5 ps (for MIPs) and corresponds to the time elapsing from the ionizing interaction to the beginning of the drift effect (plasma relaxation time). From the graph it can be seen that the total current pulse has a two contribution: Electron current having initial amplitude of 1.7 µA lasting 2 ns and an hole current having 0.8 µA at time 0 and 4 ns duration. Using a traditional charge integration readout electronics the rise-time of this pulse is above 3 ns. The 5 ps rise-time of the pulse it is somehow ideal because in reality is limited by the RC product of the input impedance of the preamplifier; namely C is the sum of detector capacitance, stray capacitance and preamplifier input capacitance that for bump bonded pixel detectors may reach values below 1 pF and R is the input ohmic resistance of the preamplifier that may go below 100 Ω in low impedance current amplifiers. Another limiting factor of this rise-time is the bandwidth of the preamplifier that for pulses below 100 ps should be above 3.5 GHz. For this reason the specification of our preamplifier should be input impedence of ≈ 50 Ω with total capacitance below 1 pF and bandwidth of about 5 GHz.

The second pillar of this approach is low temperature operation (in the order of -20°C to -40°). Low temperature operation has two advantages : (a) it reduces noise due to the leakage current of the detector and to the electronics (σ_N in equation (1)) and (b) increases mobility of the charge carriers. In the current readout configuration having higher mobilities does not impact on the rise-time (like in charge integration readout) but it shorten the overall current pulse increasing the actual amplitude (A_V in equation (1)) because the integral of the pulse is the generated charge which is a constant. In summary low temperature operation increases the Signal-to Noise ratio that reduces the time resolution. Nowadays the main LHC experiments (ATLAS and CMS) have already the infrastructures to operate vertex detectors below -20 °C,

for radiation damage reasons, therefore this fact can be exploited in the operation of these detectors.

The third pillar is the high Voltage biasing of the detector. Like the increase of mobility due to low temperature, high voltage biasing contribute to shorten the current pulse increasing its amplitude, the resulting increase in leakage current is compensated by the low temperature operation. A biasing field in the range between 10^4-10^5 V/cm is foreseen for the biasing of these detectors.

In order to complete the front end chip, after the current preamplifier also an appropriate current to voltage insertion amplifier and a discriminator should be added. The insertion amplifier should have two output channels: the first should be connected to the discriminator used as a time pickoff (Constant fraction discriminator (CFD) or Amplitude and rise time compensated discriminator (ARC) should be considered for this design) and the second should be sent to a time over threshold ADC.

3. Results from the COSIDE experiment

Although this approach is alternative to the two approaches described in section 1, it is actually not new. The author of this paper has already explored this approach in the early 90s as shown in ref. [9] in a research project named COSIDE, aiming at the construction Silicon detector based time-of-flight demonstrative detector, operating at variable temperatures in the range from 20°C to -55 °C. The analog readout chain included a current preamplifier and an insertion amplifier that converted current to voltage having two outputs one is connected to a Constant Fraction Discriminator connected with a TDC and the other to an ADC. The current preamplifier configuration was very simple (Fig. 5), the first stage is a common-emitter transistor while the second stage is an emitter follower in current feedback configuration. The preamplifier parameters were optimized by tuning noise, bandwidth, input resistance and gain. The collector current, was optimized by using by two different voltage sources at each transistor stage. The two power supplies provides, respectively, 2 V for the first stage and 6 V for the second one. The current gain was A_I = 22 the input impedance was about 100 Ω and the bandwidth was about 150 MHz. The second stage (insertion amplifier) is a two-stage integrated voltage amplifier having an overall gain of 60, a bandwidth of 320 MHz and input and output impedance of 50 Ω, the insertion amplifier drove two lemo cables one was connected to an ADC (LeCroy 2249A) the other was connected to a Constant fraction discriminator 935 by ORTEC EG & G.

The detector (Fig. 6) had 10 strip having 2 x 20 mm^2 strip-size and 300 μm thickness (15 pF capacitance). The COSIDE detector reached a time of flight resolution of 105 ps at -55 °C (Fig 7 [10]) which corresponds to 80 ps intrinsic time resolution.

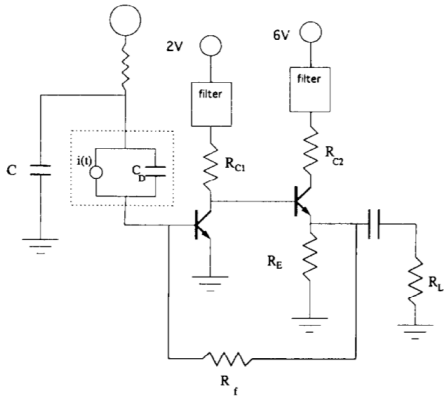

Fig.5 Front-end preamplifier of the COSIDE experiment (early 90s).

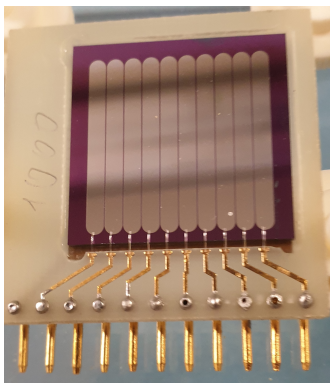

Fig.6 Silicon detector of the COSIDE experiment.

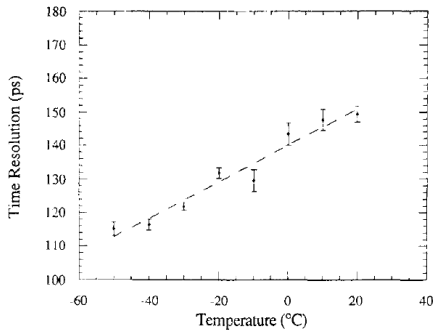

Fig. 7 Time-of-flight resolution versus temperature of the COSIDE detector.

Although the technologies used in the COSIDE detector are now obsolete the experiment demonstrated that the approach adopted is quite promising, using present pixel detector the reduced capacitance and leakage current can reduce the noise and the RC product at the input

of the preamplifier and this goes in the direction of improving the time resolution. Furthermore the use of microelectronic technologies currently used in HEP (namely TSMC 28 nm feature size) allows the possibility of a designing front-end preamplifier having adequate bandwidth (> 3.5 GHz) low input impedance (< 100 Ω) at a reasonable power consumption. Additional improvement of timing resolution is expected from the bump bonding interconnection technique because of the reduction in passive impedance of this interconnection.

4. Conclusions and outlook

An alternative approach to timing measurements using silicon pixel detectors has been proposed in this paper, this approach is based on current readout of the detector signal, low temperature (< -20 °C) of operation and relatively high voltage bias. The feasibility of this approach was demonstrated in the early 90s reaching a quite good intrinsic time resolution (in the order of 80 ps) with the technology available at that time. A large improvement of this result is expected with the usage of pixel detectors and 28 nm technical node front-end electronics.

Another important aspect of this approach is that it is based on the front end electronics optimization, while the other two approaches mentioned in this paper are based on the optimization of detectors. This opens the possibility of a combined solution that uses this approach to the front end electronics associated with one of the two detectors previously developed for timing resolution enhancement (TIMESPOT or LGAD). However since the LGAD detector current has a rise-time in the order of 0.5 ns it cannot benefit very much from the solution here suggested, while the TIMESPOT detector, that has a current pulse similar to the one shown in Fig.4 (with a total pulse duration of about 300-400 ps and an amplitude in the order of 14 μA), can have more benefits from this approach.

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