

ATLAS ITk Pixel Module Bump Bond Stress Analysis

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The upgrade of ATLAS for the high-luminosity LHC (HL-LHC) will among many detector components replace the tracking detector with an all-silicon tracker (ITk). The outer layers are composed of strip modules while the innermost 5 layers of ITk are composed of hybrid pixel modules mounted on carbon local supports.

The large temperature ranges during operation and the heterogeneous nature of the system means that thermally induced stress is present in the module bump bonds. This paper presents a model using finite element analysis of the pixel module to estimate the maximum stress in the bump bonds. Experimental results are shown of bump strength from lap-shear measurements. Finally, detailed module characterisation is presented of module bump failure due to thermal cycling. Bump bonds are demonstrated to survive 100 cycles over the design thermal cycling range with less than 0.1% thermally induced bump bond disconnects.

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1. Introduction

The Large Hadron Collider (LHC) will be upgraded to higher instantaneous luminosity (High-Luminosity LHC, HL-LHC). In the course of this, the ATLAS experiment at the LHC will also be upgraded, part of which is a replacement of the current tracking detector by an all-silicon Inner Tracker (ITk). ITk comprises four strip and five pixel layers arranged in barrels and end-caps

The ITk pixel system [1] is designed for a maximum radiation dose of about 8 MGy and particle fluence of 10^{16} 1 MeV neutron equivalent per cm^2 , without any safety factors. The pixel layers of the ITk will be composed of almost 10,000 hybrid pixel detector modules, mounted on carbon support structures. This compound structure of the detector results in a mismatch in the coefficient of thermal expansion (CTE) between components of or on the modules and the support structures. The detector will undergo temperature changes during operation which results in stress between these components, leading to a risk to the interconnection between the module components. Therefore it must be verified that the pixel detector design ensures reliable interconnections for operation over 10 years of HL-LHC.

1.1 Pixel Modules

All but the first layer of ITk Pixel will use a quad module, made up of 4 front-end (FE) ASICs, bump bonded to a sensor consisting of approx. 600,000 pixels of size $50 \times 50 \mu\text{m}^2$. The ASIC, designed by RD53, is approx. $20 \times 20 \text{mm}^2$ and the overall area of the quad module is approx. $40 \times 40 \text{mm}^2$. The pixel modules are built in two steps. The first is the hybridisation in industry, when the FE ASICs are flip-chipped to a sensor tile, producing a so-called bare module. The flip-chip process connects sensor and FE channel by channel with SnAg or In bump bonds with a pitch identical to the pixel size ($50 \times 50 \mu\text{m}^2$). The second step is the module assembly in which a flexible PCB (flex) is glued onto the bare module. The flex connects the FE ASICs and sensor to the on-detector services. The modules are parylene coated for protection against high voltage breakdown. The modules are then glued to the bare local supports, that are of different designs depending on the location in the pixel system. The bare local supports are made from low CTE material with high stiffness and are cooled. The adhesive used to fix the module to the local support has a high modulus. A cross-sectional view of a pixel module as mounted on a local support is shown in Figure 1.

1.2 Bump Bond Stress

To guarantee long term operation in the high radiation field the lowest coolant temperature of -45°C is required. This temperature both reduces shot noise and prevents thermal run-away and reduces

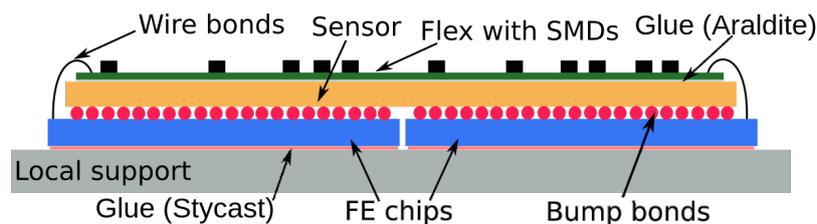


Figure 1: Cross-sectional view of an ITk pixel module mounted on a local support.

the impact of the radiation damage on the sensor current. Between operational periods, the detector can however be at room temperature. Besides the operational modes during physics data taking of the detector in the final installed configuration, several intermediate modes, particularly during assembly and commissioning on the surface and commissioning in the cavern, are possible.

All components are thus required to withstand the *operational conditions* of order of 100 cycles of the cooling system between +25 and -45°C at a rate of 1°C/min by design for ITk Pixels. Beyond the cycles due to power cuts or controlled full detector switch on/off, there is another class of thermal cycles that has to be considered. Temperature changes due to operational modes or debug purposes increase the number of cycles to up to 150, in the same operational range and speed. The modules must survive and the number of additional disconnected bumps must be less than 0.1%.

To validate the design, modules are thus cycled 100 times in an *extended* temperature range (-55°C to +60°C) and, in some setups, to a faster rate (up to 1°C/s). The extended temperature range is expected to result in earlier bump bond failures compared to the operational conditions, which allows to test to a lower number of cycles with still some safety margin.

2. Finite Element Analysis

A prediction of stress on bump bond connections and cycles to failure was obtained from a finite element analysis (FEA). The hybrid module is implemented as high density array of bumps, individually modelled with full viscoplastic material properties. The flex is modelled with realistic copper content with a Kapton layer, while sensor and FE chip are modelled with a silicon layer each of 150 μm.

From the total strain $\Delta\gamma$ on the bump bond connection, the Coffin–Manson law:

$$N_f = \frac{1}{2} \left(\frac{\Delta\gamma}{2\epsilon_f} \right)^{(1/c)}$$

allows the calculation of the number of cycles to failure N_f from the fatigue ductility coefficient ϵ_f and the fatigue ductility exponent c .

Results are shown in Table 1; they do not include creep and are based on empirical values from similar parts. These demonstrate the sensitivity of the number of cycles to failure to the copper thickness and temperature range.

	+60 → -55°C	+45 → -45°C	-25 → -45°C
25 μm Cu	2400	7700	100000
35 μm Cu	800	2600	35000

Table 1: Number of cycles to failure estimated using FEA and the Coffin-Manson model for two different thicknesses of copper in the flex.

3. Measurements

The initial strength of bump bond connections before cycling is measured in dedicated shear tests. Studies involving thermal cycling of modules through specialised machines at several sites provide

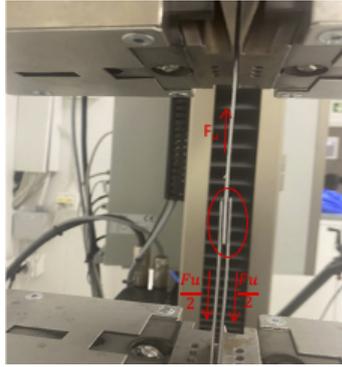


Figure 2: Picture of the double lap shear test set-up.

experimental access to the bump bond integrity of ITk pixel modules. The results of dedicated measurements with single-, double-, and four-chip modules from three bump bond vendors, denoted A, B, C, all of which are using solder (SnAg) bump material, are described in the following.

3.1 Shear Tests

The FEA described above is used to estimate the number of bump bond disconnections as a function of the number of thermal cycles and module boundary conditions. The FEA uses the ultimate shear strength of the bump bond material but the bump is more complex, being made up of under-bump metallisation (UBM) on the FE-chip and the sensor to which the bump bond connects. To provide a measurement of the ultimate shear strength of the bump bond connection, lap shear tests were carried out on several modules from two of the three considered vendors.

Bare module samples with a single and four FE chip(s) are sandwiched between a set of aluminium strips and bonded with ARALDITE 2011 adhesive. The samples are then pulled to failure via a standard pull test machine as shown in Figure 2.

As can be seen from the results in Table 2, most modules show a failure at the adhesive layer, not at bump bonds. In such a case only a lower limit of the force and the bump strength is given. In case failure is observed, the force is turned into a bump strength. A difference in bump strength between vendors A and B is observed.

3.2 Bump Defects during Thermal Cycling

Dedicated thermal cycling campaigns were carried out with the temperature changing over the extensive range of $+60^{\circ}\text{C}$ to -55°C to observe delamination faster than with the operational range as outlined above. The behaviour of the bump bond connections was investigated with double-chip and four-chip modules with Prototype (RD53A) FE chips, which are electrically half the size of the final FE chip but mechanically cut to full size, or pre-production FE chips (full size). Modules from all three vendors A, B, and C with SnAg bump bonds at the final ITk-Pixel bump bond pitch are assembled with a flex with a copper content similar to that foreseen for the production flexes. Some samples are coated with parylene. The modules are attached to different carbon sheets made of CFRP as foreseen for the end-caps (EC), Pyroid as foreseen for the outer barrel (OB) layers, or Thermal Pyrolytic Graphite (TPG).

Test	Vendor and module type	Test type	Surface preparation	Bumps per FE	Ultimate force per chip (N)	Ultimate bump strength (N)
1	Vendor-A single-chip module	Double lap shear test	Acetone cleaning	400*336	>652.8	> 0.0049
2	Vendor-A single-chip module	Single lap shear test	Plasma cleaning	400*336	>693	> 0.0052
3	Vendor-A single-chip module	Single lap shear test	Heavy acetone and alcohol cleaning	400*336	>1060	> 0.0079
4	Vendor-A single-chip module	Single lap shear test	Scotch-brite	400*336	>1450	> 0.0108
5	Vendor-B quad module 1 st FE	Single lap shear test	Scotch-brite	400*384	853	0.0056
6	Vendor-B quad module 2 nd FE	Single lap shear test	Scotch-brite	400*384	219	0.0016

Table 2: Summary of the results of lap shear-stress tests.

Between batches of several thermal cycles, the bump bond connectivity of the modules is checked by running dedicated measurements on the FE chips. Operating the modules is either carried out on a separate set-up, or inside the cycling chambers. Two types of measurements are used. For the first method the module is illuminated with a β , γ , or X-ray source while counting the registered hits in each pixel. Pixels with fewer hits compared to their neighbours or even no hits are interpreted as lost bump bond connection. The second method uses the internal charge injection circuitry of the FE chip to measure the noise or cross-talk of the sensor-amplifier-discriminator chain of each pixel. Since connection of the sensor pixel influences the behaviour of the amplifier, also these measurements provide information on the bump bond connectivity for each pixel. Given that no source is required, these measurements are easier in-situ. One of the methods using the internal charge injection is based on the change in noise Δ_{noise} between a fully reverse biased and unbiased or even slightly forward biased sensor. The variation in sensor capacity with bias voltage should result in Δ_{noise} being notably different from 0, so that $\Delta_{\text{noise}} \approx 0$ indicates a broken bump bond connection. A comparison of a measurement of Δ_{noise} with the hits as measured with a ^{90}Sr β -source is shown in Figure 3, demonstrating a high correlation between the results from both methods.

Any of these measurement methods allow monitoring of the bump bond quality as function of the number of cycles. An example of bump bond quality evolution is shown in Figure 4. The number

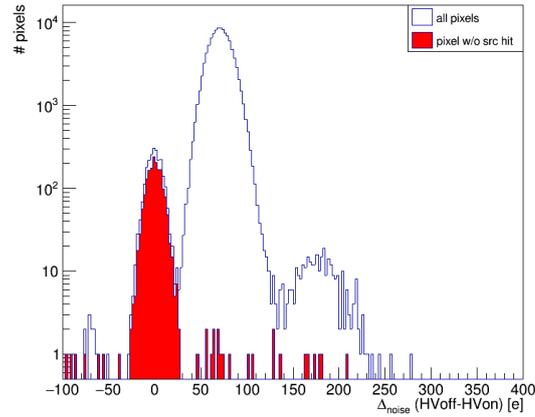


Figure 3: Histogram of the change in noise Δ_{noise} between a fully biased and unbiased sensor. The red histogram highlights those pixels that do not show any hits in a measurement with the module being illuminated with a β -source.

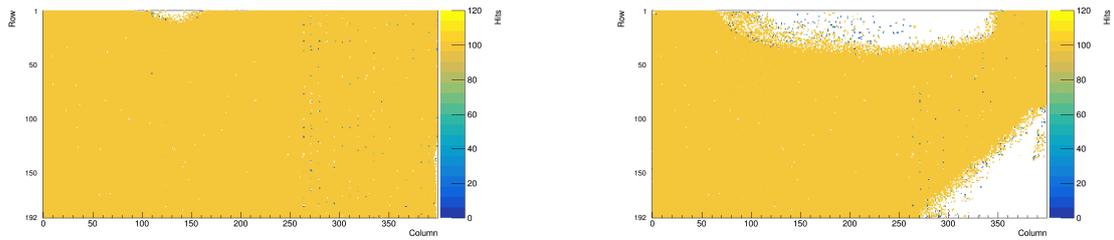


Figure 4: Map of the bump bond quality of chip 2 on module B10 based on cross-talk, with the result for each pixel colour-coded. Amber means the bump is still of good quality, white means the bump bond is disconnected. Left: status after 150 cycles; right: status after 500 cycles.

of thermal cycles before the last measurement at which the measured number of disconnected bump bonds is still below 0.1% is shown in Table 3 for RD53A-modules. That table also lists the number of cycles to which each module was exposed in total and the number of disconnected bump bonds at the end of the cycling campaign. Table 4 shows the result of modules coated with parylene without or with irradiation to a fluence of $6.3 \cdot 10^{16}$ 1 MeV neutron equivalent per cm^2 or a dose of 500 Mrad.

These measurements show that if failures are observed they occur at edges and corners of the chips. A clear difference between the vendors is observed. While one vendor shows no signs of delamination, another shows delamination before or around 100 cycles predominantly when the module is mounted on TPG support. Samples without parylene coating of the third vendor show delamination before or around 100 cycles over the extended temperature range independent of the support material, strongly growing versus the number of cycles. This behaviour is in agreement with the differences observed in the shear tests. Samples of the latter vendor with parylene coating do not show bump disconnections. The beneficial effect of the parylene coating is still observed after irradiation.

4. Summary and Outlook

The ITk that will replace the current tracking system as part of the upgrade of ATLAS for the high-luminosity LHC (HL-LHC) is composed of hybrid pixel modules in the innermost layers. Extensive studies with hybrid pixel modules were carried out to assess the behaviour of bump bond connections under temperature variations as expected during operation of ITk. These measurements confirm the simulation which expects that thermal cycling is a risk to the bump bond integrity. The measured onset of bump bond delamination depends on the vendor due to specifics of the under-bump metallisation and the bump bonds. This vendor dependency is supported by shear stress measurements. The result also depends on the carbon support material: TPG (no longer foreseen for ITk) results in earlier delamination compared to CFRP and Pyroid as foreseen for end-cap or outer barrel supports, resp. Parylene coating reduces the effect, before and after irradiation. Vendors A and C are thus qualified for modules to be built for ITk Pixel given that bump bond connections remain intact for a sufficiently large number of cycles even with a harsher cycling range. Benefiting from parylene coating allows to also go forward with vendor B. More statistics and thus more confidence in vendor B will be gained during pre-production until production. Upcoming studies with modules for the inner system (triplets of three one-chip modules) and modules with indium bump bonds, which are expected to also qualify based on FEA, will complete this campaign.

Acknowledgement

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References

- [1] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, Tech. Rep. CERN-LHCC-2017-021. ATLAS-TDR-030, CERN, 2018.

Sample	Vendor	Substrate	Parylene	Module	Chip	Number of thermal cycles with <0.1% disconnects	Max. number of cycles/number of disconnects
DCM34	C	OB TPG	no	Dual	2	50-100	500/985
GD02	C	OB TPG	no	Dual	1	10-50	700/2539
GD02	C	OB TPG	no	Dual	2	10-50	700/13594
GD01	C	EC CFRP	no	Dual	1	100-250	500/1523
GD01	C	EC CFRP	no	Dual	2	100-250	500/583
DCM32	C	EC CFRP	no	Dual	1	>1000	1000/46
DCM32	C	EC CFRP	no	Dual	2	>1000	1000/17
KEKQ14	C	OB Pyroid	yes	Quad	1-4	>100	100/0
KEKQ17	C	OB Pyroid	yes	Quad	1-4	>100	100/0
KEKQ18	C	OB Pyroid	yes	Quad	1-4	>100	100/0
GLA2	C	EC CFRP	no	Quad	1-4	>100	100/0
GLA3	C	EC CFRP	yes	Quad	1-4	>100	100/0
GLA4	C	EC CFRP	yes	Quad	1-4	>100	100/0
RD08	A	EC CFRP	no	Dual	1	>1000	1000/0
RD08	A	EC CFRP	no	Dual	2	500-1000	1000/155
RD05	A	EC CFRP	no	Dual	1	>1000	1000/31
RD05	A	EC CFRP	no	Dual	2	>1000	1000/0
RD04	A	EC CFRP	no	Dual	1	>1400	1400/26
RD04	A	EC CFRP	no	Dual	2	1200	1600/81
DCM2	A	OB TPG	no	Dual	1	>100	100/42
DCM2	A	OB TPG	no	Dual	2	250-500	1000/248
DCM5	A	OB TPG	no	Dual	1	10-50	250/354
DCM5	A	OB TPG	no	Dual	2	50-100	500/136
B10	B	EC CFRP	no	Dual	1	>50	50/0
B10	B	EC CFRP	no	Dual	2	50-100	1000/37490
B15	B	EC CFRP	no	Dual	1	500-1000	1000/855
B15	B	EC CFRP	no	Dual	2	100-250	500/41497
B17	B	EC CFRP	no	Dual	1	0-10	1000/8027
B17	B	EC CFRP	no	Dual	2	100-500	1000/11699

Table 3: Summary table of thermal cycling results for dual and quad modules. All devices have been cycled in the range -55 to +60°C. 0.1% of disconnected bump bonds corresponds to 77 bump bonds for a RD53A chip.

Sample	Vendor	Substrate	Irradiated	Number of thermal cycles with <0.1% disconnects	Max. number of cycles/number of disconnects
KEKv1-1	B	OB Pyroid	no	>100	100/0
KEKv1-2	B	OB Pyroid	no	>100	100/0
KEKv1-2	B	OB Pyroid	yes	>200	200/0
KEKv1-3	B	OB Pyroid	no	>100	100/0
KEKv1-3	B	OB Pyroid	yes	>200	200/0
KEKv1-4	B	OB Pyroid	no	>100	100/0
KEKv1-19	B	OB Pyroid	no	>100	100/0
KEKv1-19	B	OB Pyroid	yes	>200	200/0

Table 4: Summary table of thermal cycling results of vendor-B quad modules with parylene before and after irradiation. All devices have been cycled in the range -55 to +60°C. The number of disconnections after thermal cycling is given separately for the first 100 cycles before irradiation and for the second 100 cycles after irradiation. The number of total cycles is given. The irradiations were carried out at Cyric.