

## The Control System of the New Small Wheel Electronics for the ATLAS experiment

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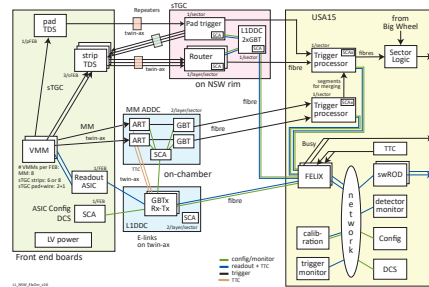
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The present ATLAS Small Wheel Muon detector will be replaced with a New Small Wheel(NSW) detector in order to cope up with the future LHC runs of high luminosity. One crucial part of the integration procedure concerns the validation of the electronics for a system with more than 2.1 M electronic channels. The readout chain is based on optical link technology connecting the backend to the front-end electronics via the FELIX, which is a newly developed system that will serve as the next generation readout driver for ATLAS. For the configuration, calibration and monitoring path the various electronics boards are supplied with the GBT-SCA ASIC and its purpose is to distribute control and monitoring signals to the electronics. Due to its complexity, NSW electronics requires the development of a sophisticated Control System. The use of such a system is necessary to allow the electronics to function consistently, safely and as a seamless interface to all sub-detectors and the technical infrastructure of the experiment. The central system handles the transition between the probes possible operating states while ensuring continuous monitoring and archiving of the systems operating parameters.

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## 1. New Small Wheel Electronics Overview

The LHC accelerator will be upgraded to deliver an instantaneous luminosity up to  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . The luminosity increase dramatically impacts the ATLAS[1] trigger and readout data rates. The present ATLAS small wheel muon detector has been replaced with a New Small Wheel (NSW)[2]. The NSW electronics for the trigger and Data Acquisition (DAQ) path of both detectors can be divided into two major categories, on-detector and off-detector electronics as shown on Fig. 1. The on-detector electronics Front-End boards, Level-1 Data Driver and ART Data Driver Card will be placed inside the cavern (detector area with radiation and magnetic fields) and consist of custom-made boards using radiation-tolerant Application Specific Integrated Circuits (ASICs). The communication between these boards will be established with the use of mini Serial Attached



**Figure 1:** Overview of the on/off-detector electronics and the DCS, Configuration and Calibration path via the SCA, the FELIX and the SCA OPC UA Server. A common readout path and a separate trigger path are developed for each detector technology. [3]

Small Computer System Interface cables. The off-detector electronics (Front End Link eXchange (FELIX), trigger processor, sector logic and services running on commercial server computers like Read Out Drivers (ROD), Detector Control System (DCS)[8], event monitoring, configuration, trigger monitor and calibration) will be placed outside the cavern in an area that is called USA15.

## 2. FELIX & GBT-SCA & SCA OPC UA Server

The keystone of the ATLAS DAQ system will be the FELIX which is an FPGA-based system housed by a commercial server. FELIX will essentially be a bridge between the front-end electronics of all ATLAS detector subsystems, and their corresponding back-end components, which will mostly be software-based. Situated in the USA15, FELIX connects to the front-end electronics of the ATLAS cavern via optical links, or GBT[5] links, each one of which is running at 4.8 Gb/s. For the NSW case, FELIX will interface with the front-end nodes over 24 optical links. These links carry the GBT frame, which is 84-bit wide. The Giga-Bit Transceiver (GBT) protocol is a transmission scheme that involves radiation-tolerant ASICs that are capable of handling the large amounts of data of high energy physics experiments. The GBT-SCA ASIC (Giga-Bit Transceiver-Slow Control Adapter)[6] is part of the GBT chipset and is usually connected both to a GBTx and to several front-end devices. Its purpose is to distribute control signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters as shown on Fig. 2. In order to meet the requirements of different front-end ASICs used in high-energy

physics experiments, it provides various user-configurable interfaces, such as SPI, I2C or JTAG, and is capable of performing simultaneous operations. In this SCA-GBTx-FELIX communication chain[3], the last two components can be viewed as data mediators, so there is one piece missing: the back end logic that actually builds the packets-to-be-transmitted to the SCA, and handles the inbound traffic from the ASIC. This is a software suite, which is a dedicated Open Communications Platform Unified Automation (OPC UA) server[7].

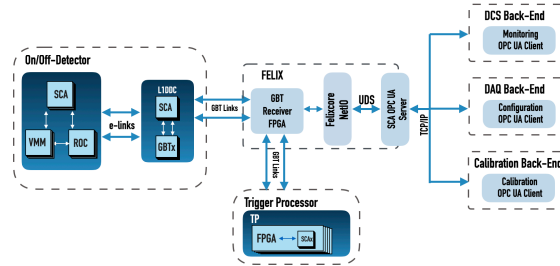


Figure 2: Overview of the calibration/configuration/monitor path.

### 3. ATLAS & NSW Control Station

The ATLAS DCS[8] has the task to permit coherent and safe operation of ATLAS and to serve as a homogeneous interface to all sub-detectors and the technical infrastructure of the experiment. The DCS must bring the detector into any desired operational state, continuously monitor and archive the operational parameters, signal any abnormal behavior. The DCS was designed and implemented within the frame of the Joint Controls Project (JCOP), a collaboration of the CERN controls group and DCS teams of the LHC experiments. Standards for DCS hardware and software were established together with implementation guidelines both, commonly for and specifically for ATLAS. It combines common standards for the use of DCS hardware based on SCADA system Siemens, WinCC Open Architecture, where it serves as the basis for all DCS applications.

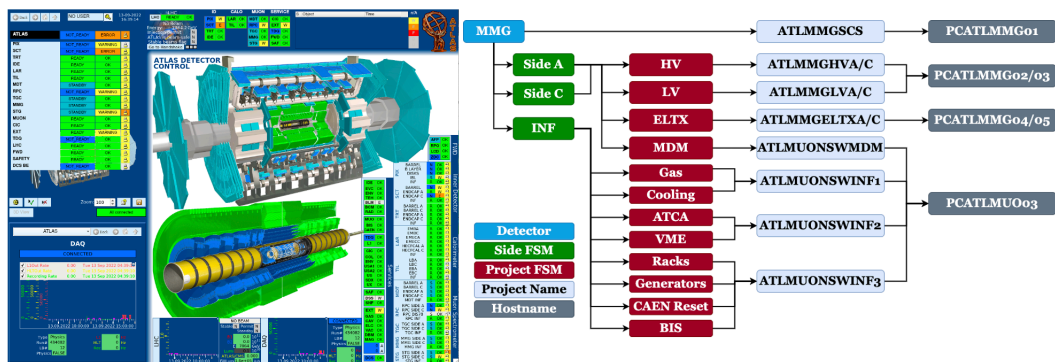


Figure 3: Left: The ATLAS Detector Control System. Right: The Micromegas(MMG) DCS structure.

Due to its complexity and long-term operation, the NSW requires the development of a sophisticated DCS. The use of such a system is necessary to allow the detector to function consistently and safely as well as to function as a seamless interface to all sub-detectors and the technical

infrastructure of the experiment. The NSW DCS architecture and its integration with the ATLAS DCS have been finalized and projects are following the existing look, feel and command structure of Muon DCS, to facilitate the shifter and expert operations. The current schema contains 2 new sub-detectors, MMG and STG. The top node of both MMG and STG propagates its state and receive commands from the ATLAS overall DCS. Currently, the NSW DCS is in the final phase of the integration into the ATLAS DCS system.

#### 4. Electronics Control Station

The ATLAS detector requires the development of an advanced DCS for the electronics monitoring using the SCA chip, which is installed on the 8000 front-end boards of the NSW. The use of such a system is necessary for the safe operation of the detector as well as to act as a homogeneous interface to all the sub-detectors and the technical infrastructure of the experiment. This system gives us the ability to monitor more than 100000 parameters which include all the power/temperature sensors, on-chip temperature and information, which are connected to the SCA on all the front-end boards of the NSW. The electronics control station has been developed, following the existing look, feel and command architecture of the other Muon sub-systems, in order to facilitate the shifter/expert operations and it is mapped onto a hierarchy of Finite State Machine (FSM) element. For each individual layer, a main panel has been developed, providing the user with useful information, reflecting the state and status of the detector, its vitals displayed in trendplots; while a secondary panel provides supplementary details. Each board's monitoring and conditions can be displayed on the panel. The state and status of the board depends on the status data point element of each board's temperature and power sensors and the communication validity of the SCA OPC UA server. The projects were validated through daily usage from shifters in the commissioning site at a first stage and then through the NSW control in the ATLAS Control room.



Figure 4: The DCS FSM and panels for the NSW Electronics monitoring.

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