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R&D status of the Selena Neutrino Experiment

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Imaging devices made from an ionization target layer of amorphous selenium (aSe) coupled to a silicon complementary metal-oxide-semiconductor (CMOS) active pixel array for charge readout are a promising technology for neutrino physics. The high spatial resolution in a solid-state target provides unparalleled rejection of backgrounds from natural radioactivity in the search for neutrinoless $\beta\beta$ decay and for solar neutrino spectroscopy with ⁸²Se. We summarize the scientific reach of a large detector with the proposed technology, and present the current status of R&D, including results from the first CMOS sensors optimized for charge collection in aSe.

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Figure 1: a) Conceptual design of the Selena Detector made from towers of large-area modules. Blue rectangles represent CMOS pixel arrays and gray areas are grounded with post-fabrication coating. b) Simulated double β tracks in the Selena Detector. Image analysis techniques can identify Bragg peaks for single/double β discrimination. The color axis in the left panel presents the number of charges collected per pixel, while in the right panel it shows the z-coordinate along the track.

1. The Selena Neutrino Experiment

The Selena Neutrino Experiment will utilize amorphous ⁸²Se (aSe) coupled to pixelated complementary metal-oxide-semiconductor (CMOS) charge sensors to probe fundamental neutrino physics [1]. Selenium-82 is one of several candidate isotopes for neutrinoless double β decay ($0\nu\beta\beta$) searches [2–6]. The spatiotemporal resolution of CMOS imaging devices allow for unparalleled background rejection in the search for $0\nu\beta\beta$ and for solar neutrino spectroscopy.

The proposed Selena Detector will consist of 5 mm of enriched aSe deposited on CMOS pixel arrays fabricated on a 300-mm diameter silicon wafer. The pixels will have a pitch of 10 μ m and a noise of 10 e⁻. Each detector module will contain ~3 kg of ⁸²Se and, by stacking the modules, the Selena Experiment will scale up to a 100 kg demonstrator, with a final goal of a 10 ton target mass. Scaling toward a large ton-scale detector takes advantage of existing industrial capabilities from the medical imaging (aSe deposition) and the semiconductor (CMOS sensor fabrication) industries. A conceptual design of the Selena Detector is shown in figure 1. Selena will achieve an environmental background-free search for $0\nu\beta\beta$ through a few techniques. First, the $Q_{\beta\beta} = 2.998$ MeV of ⁸²Se [7] is high enough such that the region of interest (ROI) sits well above most radioactive backgrounds from ²³⁸U and ²³²Th. Second, the track topology can easily distinguish between double β events, which have two identifiable Bragg peaks, and single β events. Lastly, spatiotemporal correlations between radioactive events can be used to identify and tag decay sequences [8]. This results in a final background rate of < 6×10^{-5} /keV/tn/yr [9]. With an energy resolution of 1.1% at $Q_{\beta\beta}$ [10], we estimate a 3σ discovery sensitivity of T_{1/2} = 2 × 10²⁸ yr in ⁸²Se, corresponding to $m_{\beta\beta}$ from 4 to 8 meV [11], in a 100 tn-yr exposure of the Selena Experiment.

In addition, the tagging of decay sequences can also be used to identify the unique triple-decay sequence following electron-neutrino capture by ⁸²Se, which will allow a 10-ton Selena Detector to perform background-free solar neutrino spectroscopy as well as an investigation into the "gallium anomaly," with implications for sterile neutrinos [12].



Figure 2: a) Fractional energy resolution (RMS/mean) of the 122 keV γ line from ⁵⁷Co as a function of drift electric field E_d in aSe. Our full device simulation that includes our recombination model (red line) is in good agreement with the data (black line). Blue points from Ref. [15]. b) Extrapolation with our detector simulation of the fractional resolution as a function of energy *E* up to $Q_{\beta\beta}$ at a drift field of 50 V/ μ m.

2. R&D Progress

In the coming years, the Selena Collaboration plans to build a single detector module, which involves R&D efforts on multiple fronts. In these proceedings, we report on successful results in measuring the ionization response of natural aSe (8.82% ⁸²Se) and our demonstration of the imaging of ionization events in a hybrid aSe/CMOS device. We also share the current status on the design of the TopmetalSe, a custom CMOS pixel array optimized for charge readout in aSe and fabricated on the open-source Skywater 130 nm process.

2.1 Ionization Response of Amorphous Selenium

We reported on the ionization response of aSe to 122 keV γ rays from a ⁵⁷Co radioactive source in Ref. [10]. For this measurement, we built a "single pixel" device. A layer of 200 μ m of aSe was deposited by our collaborator Hologic Inc. and sandwiched between two electrodes. We applied a high voltage (HV) via the anode and connected the cathode to the CUBE preamplifier from XGLab [13], a low-noise CMOS charge sensitive amplifier. The drift of ionized charge within the aSe induces a pulse in the CUBE, which allowed us to reconstruct the energy deposited and depth of interaction. The data acquired in this study were reproduced with GEANT4 [14], incorporating charge carrier transport and a recombination model. We reported results on the charge carrier properties and energy resolution of aSe as a function of the applied HV, shown in figure 2. We extrapolated the energy resolution to obtain 1.1% RMS at $Q_{\beta\beta} = 2.998$ MeV. These results inform the science reach and design of the Selena Detector.

2.2 Topmetal-II⁻ Prototype Coupled to Amorphous Selenium

A prototype hybrid aSe/CMOS device was made from 500 μ m of aSe, deposited by Hologic Inc., on the Topmetal II⁻ CMOS charge sensing pixel array [16]. The Topmetal II⁻ consists of a 72 × 72 array of 83- μ m pitch pixels, each containing a charge sensitive amplifier (CSA) and a *topmetal* layer as input. The *topmetal* is the 25 × 25 μ m² area of the exposed topmost metal in the CMOS stack, and is surrounded by a pixel guard ring. We used a thin gold electrode, deposited by Hologic on the top of the aSe, to apply the HV to drift charge toward the pixel array.



Figure 3: a) Frame-by-frame pixel response of Topmetal-II⁻ to a 122 keV γ from ⁵⁷Co. The pixel hit appears in Frame 1 and disappears in subsequent frames with the decay time of the CSA. **b**) Distribution of pixel values in the reconstructed event frame, showing the pixels with charge as well as the noise distribution with RMS width of 23 e⁻. **c**) Single β tracks from a ⁹⁰Sr source. The darkest pixels collect the most charge and are located at the Bragg peaks near the end of the tracks. The pixel pitch is 83 μ m.

The device was read out with a rolling shutter, where each individual pixel output is continuously multiplexed onto a single channel. An external FPGA controlled the clocking of the rolling shutter, which ran at a 25 MHz pixel rate (~5 kHz frame rate). The FPGA also monitored the array output in order to trigger our high resolution digitization. A single data acquisition event contained up to six frames, including a frame for the pixel baselines prior to the ionization event. We measured the device response to 122 keV γ rays from ⁵⁷Co and imaged single β tracks from a ⁹⁰Sr source.

Figure 3 shows a summary of our results at a field of 4 V/ μ m. These results demonstrate, for the first time, single-particle imaging in a hybrid aSe/CMOS device. We report the noise in the baseline values of the pixels to be ~23 e⁻. We were unable to reconstruct the ⁵⁷Co full energy peak due to the small area of the pixel *topmetal* electrode in relation to the total pixel area. This resulted in a decrease in the charge collection efficiency, degrading our measured energy spectrum. Charge collection can be improved by biasing the surrounding guard ring to focus the electric-field lines on the *topmetal* electrode. However, Finite Element Analysis (FEA) simulations showed that the guard ring bias required to significantly improve collection efficiency would lead to breakdown across the dielectric between the guard ring and the *topmetal* electrode. We note this as a limitation of Topmetal-II⁻, since it was not designed for charge readout in aSe.

2.3 TopmetalSe CMOS Pixel Array

The TopmetalSe is a low-noise pixelated CMOS imager for charge readout in aSe. The imagebased background suppression techniques required for the science goals described in section 1 set the design specifications of 10–15 μ m pixel pitch with 10–15 e⁻ noise. The in-pixel circuitry will include a CSA for its low-noise capabilities, an in-pixel analog-to-digital converter (ADC) for scalability, and a time-of-arrival (TOA) measurement for 3D track reconstruction. While the final readout module will be on a large diameter wafer, the prototyping of the TopmetalSe is being done





Figure 4: a) Single pixel CSA response (average waveform in black) from repeated charge injections. We applied a trapezoidal filter (red dashed line) with a rise time of 5 ms in software. The blue histogram on the left vertical axis shows the distribution of extracted pulse amplitudes. **b)** Image of a focused bike ring light on the pixel array taken with a rolling shutter. The row in red was accidentally disconnected in the design.

in multi project wafer (MPW) shuttle runs from Efabless using the Skywater 130 nm open-source Process Design Kit (PDK) [17]. So far, we have submitted two prototype designs for tapeout, the TopmetalSe-V1, with rolling shutter output, and the TopmetalSe-DPS, which implements a digital pixel sensor readout structure [18]. We share our testing results of the TopmetalSe-V1 and are currently awaiting the delivery of TopmetalSe-DPS.

We designed the TopmetalSe-V1 to have the base functionality of the Topmetal-II⁻ in the Skywater 130 nm process, maintaining the low-noise performance, low power consumption < 1 μ W per pixel, and reducing the pixel pitch to 15 μ m. The exposed *topmetal* electrode is 8.2 × 8.2 μ m² in area, surrounded by a guard ring 0.8- μ m wide. Through FEA simulations of the pixel geometry, we determined the base charge collection efficiency of ~65%, which can be improved to 99% by minimally biasing the guard ring (<10% of HV). This prototype contained a 100 × 100 pixel array with rolling shutter readout, and a few smaller test structures.

The guard ring also allows us to test the in-pixel CSA through charge injection via its parasitic capacitance with the *topmetal*, which is given by the integrated circuit (IC) design software as 3.1 fF. We used an external FPGA for the pixel selection and an external bias board for biasing the CSAs. After selection of a single pixel, we observed the CSA response to the injection of charge via the guard ring. We then applied an optimal trapezoidal filter in software and extracted the signal amplitude. The mean and RMS of the signal amplitude over repeated charge injections give us the charge conversion gain and equivalent noise charge (ENC). By injecting 50 mV pulses (967 e^-), we measured a charge conversion gain of ~20 μ V/e⁻ and an ENC of ~15 e⁻, shown in figure 4. We also share an image taken via the ionization of charge inside the CMOS substrate, which was done using an external light source focused on the pixel array. These results demonstrate the functionality and low-noise performance of TopmetalSe-V1, which we plan to couple to aSe next to demonstrate X-ray spectroscopy with improved charge collection.

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