PROCEEDINGS OF SCIENCE

Preliminary design of waveform digitizer for Jinping neutrino experiment at CJPL

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Abstract: This paper reports a preliminary design of the waveform digitizer "WRX0608A1" for the Jinping Neutrino Experiment (JNE) at the China Jinping Underground Laboratory (CJPL). This digitizer includes a 6-channels compact Peripheral Component Interconnect (cPCI) board with a sampling rate of 1000 MS/s and 13-bit resolution for each channel. It upgrades the original data acquisition system and also is a key part of future 4000-channel readout electronics. Here, we report the system design and performance testing in detail. Key parameters include the effective number of bits (ENOB) being greater than 10 bits, and the quad small form-factor pluggable plus (QSFP+) high-speed signal lane being able to perform long-term error-free transmission under a bandwidth of 10.3125 Gbps. These parameters satisfy the front-end waveform digitization and high-speed data transmission requirements of the current JNE prototype and of future hundred-ton experiments. A joint debugging experiment involving a 30-channel data readout system and a prototype detector is in progress.

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1. Introduction

The proposed JNE serves to study MeV-scale neutrinos, including solar neutrinos, geoneutrinos, and supernova relic neutrinos [1]. A 1-ton detector, which is built as a prototype of the JNE at CJPL-I hall A, has been used since 2017 [2]. The target detector is spherical, and the optical signal inside the detector is read by 30 photomultiplier tubes (PMTs). The data acquisition system digitizes the electrical signal output by the PMTs, and determines whether to save the data according to the multichannel coincidence trigger. The prototype's readout electronics are based on four V1724 flash analog to digital converter (ADC) boards and a V1495 logic trigger module from CAEN, which have been used to record physical events. Next, we plan to increase the mass of the detector's target material to the order of hundreds of tons by 2026. Correspondingly, the number of PMTs and electron channels will also increase to four thousand. Limited by the bandwidth (1 Gbps) and resolution (10-bit) of the currently used readout electronics system, the acceptable trigger rate of the system is low, and the system crashes when operating at frequencies above 600 Hz. Simultaneously, to facilitate the design of the system and to upgrade, we need to upgrade the readout electronics system. Described here is the high-speed waveform digitizer for directly digitized PMT signals, which is one of the most important parts of the upgraded readout electronics system.

2. Hardware design

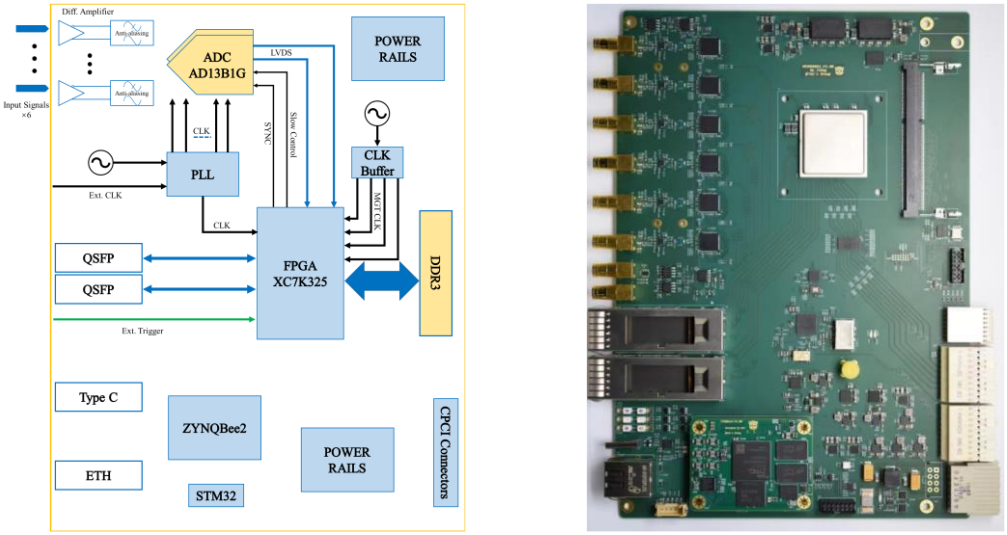

Figure 1. WRX0608A1 waveform digital system architecture diagram (left) and PCB physical photo (right).

To satisfy the needs of JNE readout electronics, especially in term of resolution and bandwidth, we designed a 6-channels 1 GSPS, 13-bit digitizer "WRX0608A1". WRX0608A1 is based on the 6U cPCI standard, with a total of 12 layers, and the board comprises inexpensive flame retardant 4 (FR-4) material. Figure 1 shows an architecture diagram and a physical photo of the printed circuit board (PCB). The ADC front-end uses DC coupling, and the anti-aliasing filter bandwidth is designed to be 500 MHz. The input signal is biased through the AD5686 digital-to-analog converter (DAC) [3] and AD8676 [4] operational amplifier. The main control chip of WRX0608A1 is Xilinx's FPGA 7k325t, and the maximum designed capacity is 4GB DDR3 cache. The custom-developed ZYNQBee2 module is used to perform slow control on the

system, including remote updating of FPGA firmware, flash memory, bias adjustment, etc. The ZYNQBee2 module is based on Xilinx's ZYNQ7010. The clock tree is designed based on TI's LMK04803 [5], and can be quickly configured through the STM32 microcontroller upon powering the system.

3. The test of waveform digitizer

Experimental testing was conducted on the power rail, DDR3, QSFP+ interface eye diagram, ADC ENOB and network port of the WRX0608A1. The QSFP+ interface eye diagram and ADC ENOB test are described in detail.

3.1 Eye diagram test of QSFP+

Table 1. Front panel QSFP interface signal integrity test

MGTX_B118 Channel	**Open Area**	**Open UI**
Channel 1	4216	53.85%
Channel 2	3904	55.38%
Channel 4	3978	52.31%
Channel 4	4543	50.77%

We tested the QSFP+ high-speed lane signal integrity based on the integrated bit error ratio tester (IBERT) IP core provided by Vivado software, and the test setup is shows in Figure 2 left. A 100G loopback module is used to perform a self-loopback test of the lane (the receiver is directly connected to the transmitter). In the test, the lane speed was set to 10.3125 Gbps and the encoding method used was a 7-bit pseudo-random binary sequence (PRBS). The test results show that the eye diagram opening area and opening UI of the four lanes are better than 3900 and 50%, respectively, as shown in Table 1. When the bit error ratio (BER) is 6.393e-15, the lane error is zero. This result supports that the QSFP+ interface can complete error-free data transmission at a bandwith of 10 Gbps.

3.2 ADC ENOB test

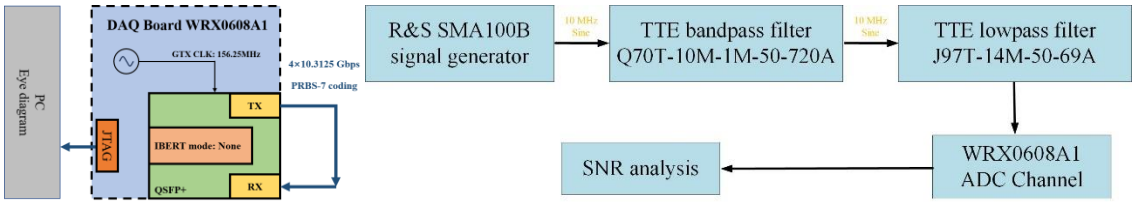

Figure 2. The test setup of QSFP+ high speed lane signal integrity (left) and the test setup of ADC's ENOB (right).

In the ENOB test, the sine wave fitting method was applied based on the IEEE-1241 standard. This process includes inputting a full-scale sine wave into the ADC, analyzing the sine wave spectrum digitized by the ADC, obtaining the signal-to-noise ratio (SNR) value, and then calculating the ENOB. The experimental setup is shown on the right of Figure 2. R&S®'s SMA100B is used as a sine wave signal generator, and its output sine wave is bandpass and low-pass filtered to reduce harmonic. The bandpass filter and low-pass filter were TTE Q70T-10M-1M-50-720A and J97T-14M-50-69°, respectively. We set the SMA100B to output a 10 MHz sine

wave, and the sampling depth is set to 65536 ns. The test analysis results of ENOB are shown in Table 2. The measurement results show that the ADC ENOB is greater than 10 bits.

Table 2. Test results of ADC ENOB at 10 MHz input.

	1	2	3	4	5	6	7	8	9	10	
Channel 2	9.86	10.02	9.93	10.00	9.85	9.79	9.93	9.75	9.89	9.92	9.89±0.09
Channel 2 + bandpass filte	9.88	9.97	9.98	10.05	9.91	9.83	9.85	9.96	9.79	9.78	9.90±0.09
Channel 2 + bandpass filte + lowpass filter	10.01	9.90	9.93	10.01	10.03	9.87	9.80	9.86	10.02	9.91	9.93±0.08

4. Conclusion

This paper describes the preliminary design of the JNE waveform digitization system. The waveform digitization system WRX0608A1 is based on six 1 GSPS, 13-bit ADCs, and the measured ENOB is greater than 10 bits, which is higher than the 8.6 bits currently used. Data transmission can be carried out through the front panel or backplane with a bandwidth of 10 Gbps, which indicates that at a memory depth of 600 ns, an average trigger rate of 186 kHz is acceptable. This performance represents a great improvement over the existing system and can satisfy the needs of future Jinping applications. The electronic requirements of micron experiments can be used as a key part of the future 4000-channel readout electronics system. In addition, the construction and testing of the 30-channel data acquisition system are in progress.

5. Acknowledgements

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