PROCEEDINGS OF SCIENCE

KM3NeT acquisition electronics: status and upgrade

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The KM3NeT Collaboration is building and operating two deep-sea neutrino telescopes at the bottom of the Mediterranean Sea. The telescopes consist of lattices of light detectors housed in pressure-resistant glass spheres, the so-called digital optical modules, which house 31 3-inches of diameter photomultipliers, as well as the acquisition electronics. The so-called detection units are vertical strings along which digital optical modules are installed. For the first phase of the construction of the telescopes, several tens of detection units have been produced, out of which almost 40 have already been deployed with more than 20,000 photomultipliers installed and taking data. Once finished, the two telescopes will have installed more than ten thousand acquisition nodes, completing one of the more complex networks in the world in terms of operation and synchronisation. This work presents the current status of the acquisition electronics, including the upgrade of the principal components such as the central logic board, the signal collecting board, switching core board and Glenair back plane.

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1. Introduction

The KM3NeT Collaboration is engaged in the construction and operation of two deep-sea neutrino telescopes located at the bottom of the Mediterranean Sea. These telescopes are designed to detect neutrino interactions by using lattices of light detectors contained within pressure-resistant glass spheres known as Digital Optical Modules (DOMs) [1]. Each DOM houses a cluster of 31 3-inches of diameter photomultiplier tubes (PMTs) distributed on the surface of the glass sphere, and the necessary acquisition electronics inside. DOMs are installed along vertical strings called Detection Units (DUs). There are 18 DOMs per DU. In the initial phase of telescope construction, a considerable number of DUs have been manufactured, and almost 40 of them have already been deployed, incorporating over 20,000 installed PMTs that are actively collecting data. Once fully completed, the two telescopes will have an intricate network comprising over ten thousand acquisition nodes, establishing one of the most sophisticated operational and synchronised networks worldwide. This paper provides an overview of the current status of the acquisition electronics in the KM3NeT neutrino telescopes [2–4]. Emphasis is placed on the ongoing upgrade of key components, the so-called: central logic board [5, 6], signal collecting boards, switching core board and Glenair back plane. The upgraded electronics will enhanced data collection capabilities, improving the overall performance and efficiency of the data acquisition system of the telescopes. The work presented herein highlights the progress made so far in the electronic boards of the development of the KM3NeT neutrino telescopes.

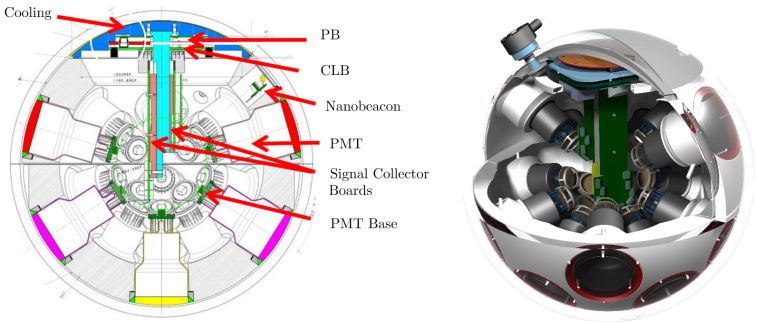

Figure 1: Left: 2D vertical cross section of the DOM with the main components indicated. Right: 3D representation of the DOM.

2. KM3NeT hardware

The DOM is the main element in the KM3NeT telescope operation. The 31 PMTs and all the necessary electronics to control the operation of the DOMs are located inside. The principal electronic board is called the Central Logic Board (CLB), which manages and controls all the functionalities of the DOM. Connected to the CLB there is the Power Board (PB), whose mission is to generate all the voltages required by the DOM. The PMTs are connected to boards called bases, which are responsible for generating the power supply voltage for the PMT, as well as digitising its electrical signal to be sent to the CLB. The signals from the PMTs are sent to the CLB for processing by means of two boards known as the Signal Collector Boards (SCBs). Finally, all the

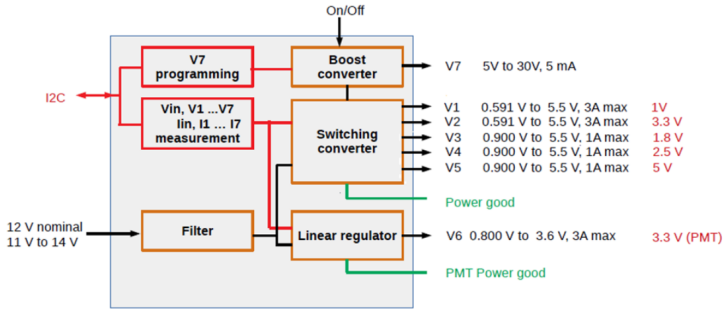

Figure 2: Block diagram of the power board. From a 12 V input voltage, all the necessary voltages for the operation of the DOM are generated using voltage regulators.

DOMs incorporate a device called Nanobeacon for time calibration, which uses a pulsed LED [7]. Figure 1 shows a representation of the DOM with the position of all its componentes.

2.1 Central Logic Board

The CLB, [8, 9] is a multi-layered electronic board that controls the functioning of the DOM, including acquisition, synchronisation, instrumentation, and various communication interfaces. The control of all the components of the electronic board is implemented on a Field-Programmable Gate Array (FPGA) Kintex-7 from Xilinx Inc. The FPGA is responsible for the acquisition and processing of the optical signals generated by the PMTs, and the acoustic signals collected by the piezoelectric sensor of the positioning system. The CLB includes the acquisition firmware and the embedded software [10, 11]. All events, both optical and acoustic, are digitised with a timestamp provided by the White Rabbit (WR) synchronisation protocol. This protocol enables the synchronisation of all the KM3NeT nodes with an accuracy of 1 ns.

2.2 Power Board

At the entrance of each DOM, there is a voltage converter that transforms the voltage signal of 375 – 400 V DC from the high-voltage power supply system of KM3NeT into a 12 V DC voltage. The PB receives these 12 V and generates all the voltages required by the DOM: 1 V, 1.8 V, 2.5 V, two 3.3 V (one for the CLB and another for the PMT power supply), 5 V, and an adjustable voltage between 5 – 30 V for the calibration systems [12]. If all the voltages have been generated correctly, a signal called Power Good is activated. Two analog-to-digital converters (ADCs) are used to read all voltage and current values. Figure 2 shows a descriptive diagram of the PB with all its power supplies and configuration interfaces.

A previous study was conducted to accurately select the voltage converters, taking into consideration the current requirements for each power supply rail. This allowed for the optimisation of the board's efficiency. The total power consumption of a DOM is approximately 6 W. The PB incorporates a sequential start-up of the voltages, ensuring proper power supply to the FPGA. This prevents excessive currents during start-up that could damage the system.

2.3 Signal Collector Board

The Low voltage Differential Signals (LVDSs) generated by the PMTs bases are sent to the CLB by two SCBs. The first one, called SCB Large, sends the signals of the 19 PMTs located in the lower hemisphere of the DOM, and the second one, called SCB Small, sends the signals of the 12 PMTs located in the upper hemisphere. The SCBs are also responsible for sending configuration and monitoring commands from the CLB to the PMTs. The main components of the SCBs include a Molex 754332104 connector, a Xilinx Coolrunner Complex Programmable Logic Device (CPLD) chip for controlling and monitoring the PMT bases through current sensors, current limiters, a multiplexer for different Inter-Integrated Circuit(I^2C) lines, and a link that allows communication between the acoustic piezoelectric sensor and the CLB.

3. Upgrade and new developments

3.1 Central Logic Board

The CLB has been designed to include a total of 12 layers, comprising 6 signal layers, 2 power planes, and 4 ground planes. These layers are arranged symmetrically around the 2 power planes. The positioning of the ground planes alongside the signal layers was done to enhance signal integrity. Special attention was given to routing the differential pairs in order to maintain a time difference of less than 100 ps between different PMT signals and less than 20 ps between clock signals. A reliability analysis was conducted using the FIDES method [15], which indicated an estimated failure risk of less than 10% over a span of 15 years. Various signal integrity simulations were performed on different signals present on the board, demonstrating a high level of discrimination. Several modifications have been made regarding the original board. One of the most important has been the provision of a secondary clock circuit. Since KM3NeT is an isolated system that cannot be repaired or modified when in operation, if the clock system fails, the DOM would be completely lost. This is why it has been decided to include a backup clock system. Figure 3 shows a diagram of the complete clock scheme of the upgraded CLB. Another challenge faced by an experiment whose construction can last several years is component obsolescence. Several components in the CLB have already become obsolete, being the most important one the Molex connector that connects the CLB with the signal collector boards. A redesign of the electronic board has been necessary, replacing the Molex connectors with another combination of SAMTEC connectors specifically designed for KM3NeT. Figure 4 shows a 3D representation of the upgraded CLB design.

3.2 Signal Collector Boards

Also, the SCBs have been affected by the obsolescence of components, which has led to a redesign of the electronic board. Similarly to the CLB, the main obsolescence problem in the SCBs has arisen with the Molex connector that connects them to the CLB. A change to SAMTEC connectors with a specific configuration for KM3NeT has also been necessary for these boards. A model with the CLB and the signal collection boards integrated in the mechanical frame of the DOM is shown in Figure 5.

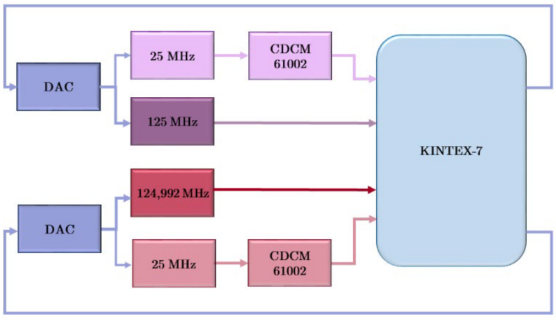

Figure 3: Block diagram of the clock system of the upgraded version of the CLB, including the main clocks and the backup circuit based on 25 MHz and CDCM61002.

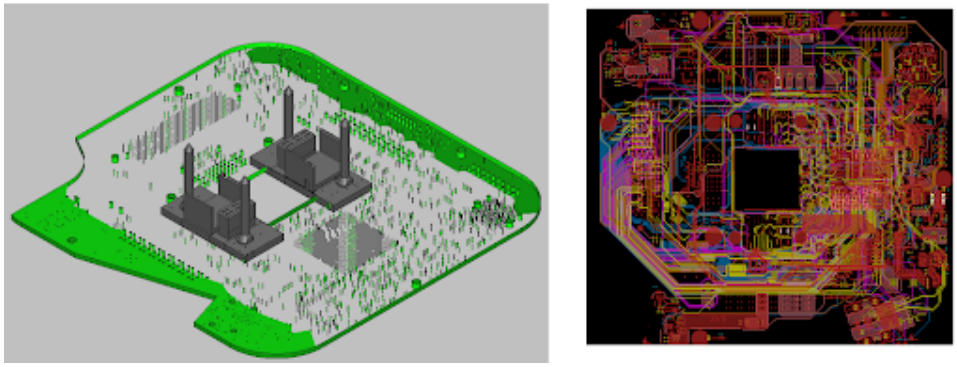

Figure 4: 3D model (left) and layout (right) of the upgraded CLB.

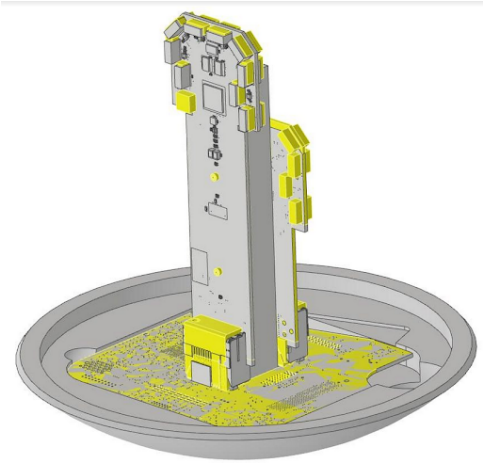

Figure 5: Mechanics model where the upgraded versions of the CLB and the SCBs are integrated into the mechanical support of the DOM.

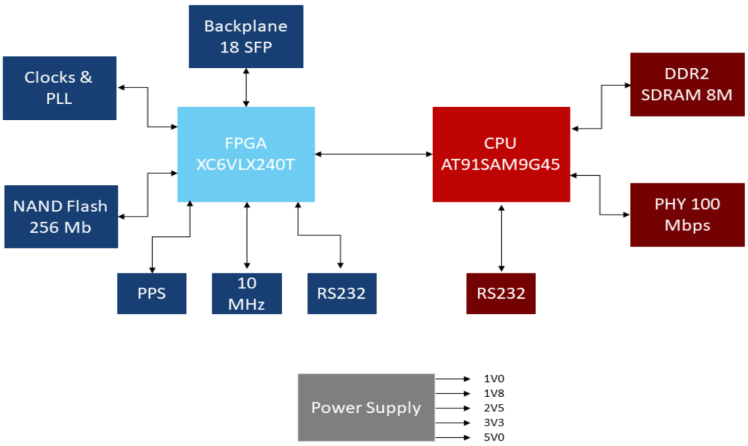

Figure 6: Diagram of the main blocks that form the so-called White Rabbit Switch.

3.3 White Rabbit Switch

The KM3NeT experiment is an infrastructure composed of thousands of DOMs, which are responsible for detecting and processing the Cherenkov radiation induced by the charged particles produced in the neutrino interactions, to reconstruct the trajectory and energy of these neutrinos. The DOMs, separated by tens of meters, have their own acquisition electronics and their own temporal scale, so it important to synchronise the clocks of all DOMs with high precision. To achieve this, the White Rabbit (WR) protocol has been used [13, 14]. WR forms a hierarchical network topology designed on top of the Ethernet physical layer, based on bidirectional timeTransmitter - timeReceiver links, where the timeReceivers nodes are the DOMs and the timeTransmitters are the White Rabbit Switches (WRSs). This device allows to combine both synchronisation and data packets on the same physical connection medium. It consists of two electronic boards: the SWitching Core Board (SWCB) and the back plane. Figure 6 shows a diagram of the WRS with its main functional blocks.

3.3.1 Switching core board

The main hardware of the WRS is the switching core board. It is implemented in the microTCA standard, which is a compact standard with a redundant power supply, remote control, and designed to support high data rates. Due to the compact size of the microTCA standard, the optical connectors of the 18 ports are incorporated on another card that is attached using two QSS-048-01-LD-DP connectors. A reliability study was conducted based on the FIDES method, which revealed that the components that contributed the most to increasing the device's failure rate, known as FIT (Failures In Time), were the decoupling capacitors. As a result, an upgrade of the board was performed by selecting new capacitors that improved the ratio between their maximum voltage and the voltage at which they operate in the WRS. This new component selection will reduce the failure rate by a 66%. The testing of the produced switching core boards has also been enhanced. The main goal is to improve the reliability. The testing tool developed for the automatic test of the switching core boards is shown in Figure 7.

Figure 7: System test for the functional test of the switching core boards. The automatisation of the production is of crucial importance for increasing the reliability of the boards to be used in the experiment.

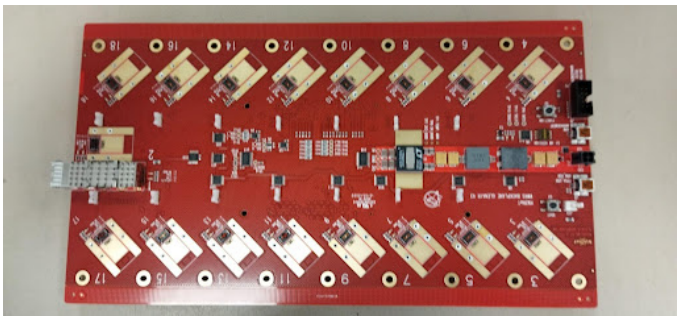

Figure 8: New design of the Glenair back plane adapting the geometry to KM3NeT requirements and including the new optical transceivers from Glenair.

3.3.2 Glenair back plane

The other electronic board that forms the WRS is called the back plane. It incorporates 18 Small Form-factor Pluggable (SFP) optical fiber transceivers. In the case of KM3NeT, due to space constraints, power consumption, and reliability requirements, a new design was necessary. The board was designed with a different geometry and with different optical transceivers from the Glenair company, which provide improved reliability and power consumption. This new board, called the Glenair back plane, is shown in Figure 8.

4. Conclusions

The main electronic boards of the KM3NeT experiment and their basic operation within the experiment have been presented. The main upgrades of these boards have been described, as well as the main redesign criteria such as higher efficiency, improved reliability, or component obsolescence requirements. The modifications and enhancements implemented have significantly improved the

overall reliability and performance of the KM3NeT experiment. These advancements have been adapted to obsolescence ensuring the performance and minimising failure rates.

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