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The TDAQ system of the HEPD-02 on the CSES-02 mission

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The High-Energy Particle Detector (HEPD-02) is a particle spectrometer developed by the Italian collaboration Limadou within the CSES-02 mission. It has been designed for the detection of electrons (3-100 MeV), protons (30-200 MeV), and light nuclei, in the near Earth orbit. HEPD-02 is the first detector to use a pixel silicon tracker in space. The Monolithic Active Pixel Sensors (MAPSs) constituting the HEPD-02 silicon tracker are characterized by excellent spatial resolution, lower production costs, higher robustness, and lower noise when compared to traditional microstrip sensors. Nevertheless, stringent requirements on power consumption for space applications lead to a challenging optimization of power demanding processes. Within this paradigm, a tailored Tracker Data AcQuisition (TDAQ) system has been designed. The TDAQ firmware was developed on a Field Programmable Gate Array (FPGA) manufactured by Xilinx: a low-power version of the Artix family with a suitable amount of resources. The parallelization implemented within the TDAQ algorithm was a crucial point in optimizing the limited read-out speed, imposed by power constraints. Nonetheless, the strengths of the TDAQ firmware consists in its modularity and redundancy. In this work, we will present the characterization and the performance of the HEPD-02 TDAQ system.

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1. Introduction

The China Seismo-Electromagnetic Satellite (CSES) [1, 2] is a scientific space mission devoted to monitoring electromagnetic, particle and plasma environment in the near-Earth region. CSES is part of a collaboration between China National Space Administration (CNSA) and the Italian Space Agency (ASI) involving numerous Universities and research institutes. The motivations of the CSES program consist in the investigation of of atmosphere and inner van Allen belts perturbations originated by solar [3–5] and terrestrial phenomena. CSES searches for a statistical correlation between such transient and seismic phenomena, as indicated by previous analyses on Particle Bursts (PBs) [6, 7]. Having measurements and monitoring instruments in place allows for the collection of data necessary to validate models. Another objective of the mission consists in the study of low energy cosmic rays: electrons in the range 3-100 MeV and protons in the range 30-200 MeV.

The first satellite, CSES-01, was launched in 2018, while another one, CSES-02, is currently in the integration phase. Among the payloads hosted by CSES-02, there will be the High Energy Particle Detector (HEPD-02), built by the Italian *Limadou* collaboration. HEPD-02, an upgraded version of the predecessor HEPD-01 onboard CSES-01 [8], is a particle spectrometer able to perform event-based Particle Identification (PID) thanks to the interplay between its different subdetectors: plastic scintillator trigger planes, three layers of silicon pixel tracker, a segmented calorimeter made of plastic scintillator, an inorganic calorimeter made of LYSO (Lutetiom Oxyortho Silicate), and an Anti Coincidence Detector (ACD) made of plastic scintillator. In figure 1, it is possible to see the detector assembly with its components.

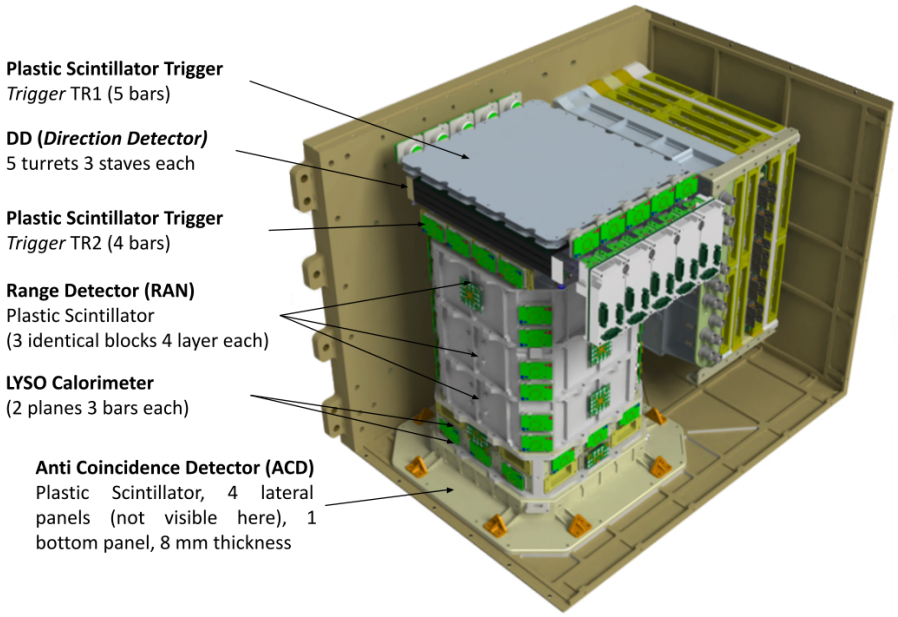

Figure 1: The HEPD-02 assembly onboard CSES-02 with its sub-detectors: trigger planes, silicon pixel tracker, plastic scintillator tower, LYSO calorimeter, Anti Coincidence Detector (ACD).

HEPD-02 is the first detector to use a pixel silicon tracker in space [9], and as such, it represents an important advance in particle spectrometry. In comparison to conventional microstrip sensors,

the Monolithic Active Pixel Sensors (MAPS) used in HEPD-02 provide superior spatial resolution, cheaper production costs, improved robustness, and lower noise. A custom-designed TDAQ system has been implemented to satisfy the strict power consumption requirements of space applications. The TDAQ firmware established a delicate balance between optimization and scalability by utilizing a low-power Field Programmable Gate Array (FPGA) from the Xilinx Artix family. The parallelized architecture implemented the TDAQ firmware proved essential in maximizing the read-out speed while respecting the power limits. Furthermore, the TDAQ firmware is notable for its adaptability and redundancy, which improves its versatility and dependability.

We will discuss the characterization and performance evaluation of the TDAQ system integrated into HEPD-02.

2. Hardware hierarchical architecture of the HEPD-02 instrument

The HEPD-02 payload is composed by different subsystems. The Detector Subsystem (DES): this subsystem comprises all the detectors mentioned in the previous section. The the electronic boards handling triggers, data acquisition and processing are grouped within the Electronics Subsystem (ELS) consisting of:

- Direction Detector [9–11] (or Silicon Pixel Tracker) Data Acquisition Board (T-DAQ)
- Trigger board (TRIG) [12, 13]
- Data Processing and Control Unit (DPCU) [14]

The DES and ELS are then feeded by the Power Supply Subsystem (PPS) consisting of:

- Low-Voltage Power Supply (LVPS) with the Low Voltage Control module (LV-CTRL) and the Low-Voltage DC/DC converter module (LV-DCDC)
- High Voltage Power Supply (HVPS) with the High Voltage Control module (HV-CTRL) and 16 High-Voltage DC/DC converter modules (HV-DCDC)

3. The Silicon Pixel Tracker of the HEPD-02

The HEPD-02 Direction Detector (DD) [10], consisting of 150 ALTAI Monolithic Active Pixel Sensors (MAPS) in total, will be the first silicon pixel tracker ever used for space-based applications. ALTAI chips are fabricated by Tower Semiconductor LTD with a 180 nm CMOS process. The choice of this silicon pixel sensor was guided by several criteria: very good resolution (pixel size of 28 μm $\times$ 28 μm), low material budget (the silicon substrate can be thinned down to 100 μm or even 50 μm), low noise, low power consumption ($<$ 19 mW/cm^2).

The DD has been developed with a hierarchical architecture displayed in Figure 2. The fundamental block of the DD is the *stave*: 10 ALTAI MAPS chips, organized in two columns of 5 chips each, are soldered onto a Flexible Printed Circuit (FPC), forming the so called Hybrid Integraded Circtuit (HIC). Stiffness and thermal drain are then provided by the carbon fiber reinforced polymer structure [11]. Then, the *turret* is assembled by stacking three staves together and by connecting them to the control/readout electronics via the Track Splitter (TSP) board. The overall tracker is then obtained by placing 5 *turrets* side by side.

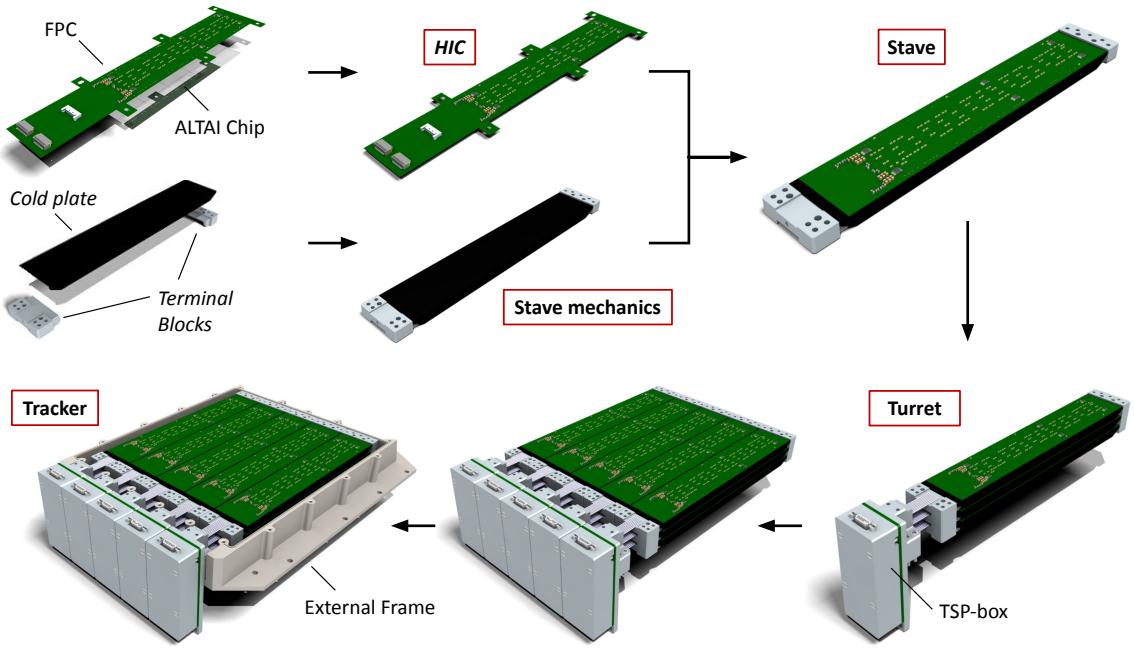

Figure 2: Visualization of the Direction Detector (DD) assembly. The tracker is composed 5 *turrets*. In each *turret*, 3 *staves* are stacked and connected to the Track Splitter (TSP) board. Each *stave* contains 2 columns of 5 ALTAI MAPS chips each.

4. The Tracker Data AcQuisition (T-DAQ) board

The ALTAI chip sensor features both a fast Serial Data Transmission module, with 1200 Mbps / 400 Mbps serial out port, and a relatively slower (40 Mbps) Control Logic Bus module, through which it is possible to both configure the chip and access the data on it. Operating the ALTAI sensor with the fast serializer module (consuming approximately 70 mW per chip) would easily overshoot the power budget for the HEPD-02 DD. Given the low event rates expected for HEPD-02, it turns out that, the limited speed of the configuration port (Control Bus Logic) is sufficient for the on-flight operations. In this way, the fast serializer can be kept switched off drastically reducing the power consumption of each ALTAI sensor.

Figure 3 schematically shows the structure of the T-DAQ board, the connections between the tracker and the board, and a simplified sketch of the implemented firmware. ALTAI chips are operated with the use of two differential lines: a M-LVDS DCLK line for clocking the digital section of the sensor at 40 MHz and a DCTRL M-LVDS bidirectional serial line for synchronous communication. As mentioned before, the high speed serial line is not used for power consumption constraints. The DCTRL line is used to deliver the trigger signal and then to readout the active pixel location. To achieve a sufficient readout speed, the TDAQ implements a separate firmware module for each stave. For each trigger, the staves are then interrogated in parallel for possible hit data.

In the HEPD-02 tracker architecture, each stave contains two master ALTAI chips, each one communicates with 4 ALTAI slaves, for a total of 10 ALTAI chips. T-DAQ send commands and performs the read-out, via the master chips, using the *control module* (CTRL in figure 3). To reduce the power consumption the ALTAI chips are usually kept in a idle state, obtained by switching

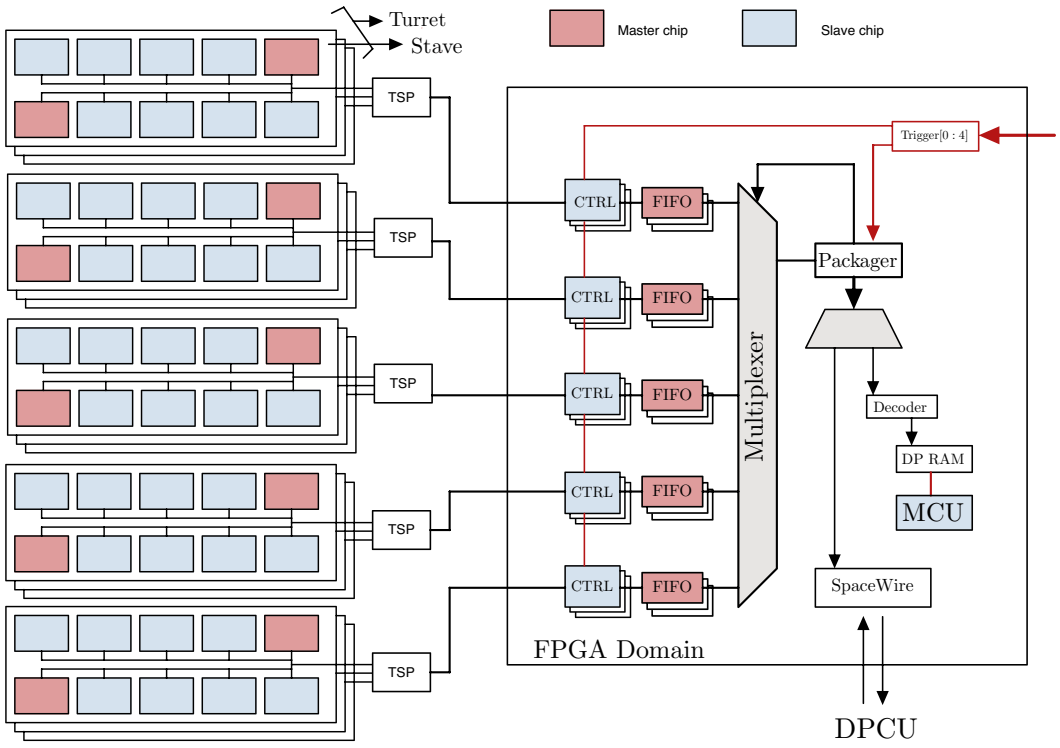

Figure 3: Schematical view of the tracker with the connections to the T-DAQ board. The internal architecture of the T-DAQ firmwer is depicted on the right.

off the clock signal generated by the TDAQ. Whenever a trigger is generated, the TDAQ is also informed about which scintillating tile of TR1 is activated. Correspondingly the TDAQ enable the clock only for the tracker turrets matching geometrically with the TR1 signals.

From the point of view of the general DAQ, T-DAQ is a slave component of HEPD-02. This means that the T-DAQ platform responds only when a command or a trigger is delivered from the outside (i.e. instructions from the DPCU or triggers from Trigger board). T-DAQ operates in two modes: Idle and Data acquisition mode. In the Idle mode, T-DAQ executes commands from the DPCU, but ignores any trigger signal (i.e. the busy signal is continuously asserted). This mode is used for diagnostics, ALTAI sensor calibrations and configurations. In the Data acquisition mode, T-DAQ waits for trigger signals eventually delivered to the corresponding turret. Then, the firmware embedded in the FPGA collects the data from the ALTAI chips from the different staves, prepares the data package, and writes the data packet on the output buffer.

All the communications between T-DAQ and DPCU, with also the data transfer, are implemented exposing a shared memory area, using a Dual-Port RAM (DPRAM). Then, the DPCU will send commands to the T-DAQ by writing the command at the designated memory address. The writing and reading procedures are performed using a custom protocol, on top a Space Wire Light links.

5. T-DAQ Power Consumption and Performances

The power consumption for the ALTAI sensors, operated in an equivalent *slave mode* is kept below 71 mW per chip. An accurate characterization of the tracker power consumption has been performed with a prototype of the tracker power supply unit (T-PSU: an accurate reproduction of the power supply circuit on the LVPS board), and a bench power supply unit (PSU) for generating the negative bias tension (V_{EE} = -4 V), not delivered by the T-PSU.The bias line has only to deliver the leakage current of the junctions, below 2 mA per stave. For the sake of the overall power consumption, the contribution for the bias current is negligible. In addition, for the HEPD-02 Flight Model (FM), only the staves with the lowest power consumption on the bias line were selected.

In the Tracker design, power saving is also achieved by adopting clock gating, i.e. clock is delivered to the ALTAI sensor chips only when a trigger is received and is enabled only for the necessary read-out time. Moreover, when the clock gating feature is disabled (and therefore clock is always enabled), the power consumption of the chip is constant. For the setup with one turret, the Tracker-PSU, and the Bench PSU, it has been observed that, in clock enabled condition, the power supply was about 3.2 W, while, in clock switched off condition, the power consumption decreased at about 1.6 W. Clock gating allows for the possibility to increase the absorbed power of the system, for a very limited time only (the readout time). Therefore, this operation mode will translate into a dependence of the averaged power consumption as a function of the trigger rate. It has been estimated that the entire tracker system will have a power consumption below 9 W at about 600 Hz of trigger rate, and below 10 W at a trigger rate of about 1.2 kHz.

6. Conclusion

The Direction Detector of the HEPD-02, onboard CSES-02, will be the tracker using CMOS Monolithic Active Pixel Sensors (MAPSs), specifically ALTAI chips, customized for space applications. The ALTAI sensor's low material budget and fully digital integrated readout make it highly desirable for space-based instruments. To fit within the tracking system's limited power budget of around 10 W, smart strategies were implemented in the DAQ design. T-DAQ was specifically developed to address the issue of tracker power consumption by parallelizing and pipelining the readout with FPGA-based firmware. In particular, parallelization effectively addressed the limited data transfer bandwidth caused by the slow serial control port of the ALTAI chip. Furthermore, extensive use of clock gating significantly reduced dynamic power consumption. Additionally, leveraging the versatility of FPGA firmware design, a soft-core Microcontroller Unit (MCU) has been implemented for ALTAI chip calibrations and configurations.

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