PROCEEDINGS OF SCIENCE

Operation and Performance of CMS Pixel Detector

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The CMS pixel tracker provided high-quality physics data during the LHC Run 2, finishing with a detector live fraction of 95% and hit efficiency of >99% in all but the innermost layer. However, issues encountered during Run 2 - in particular direct current to direct current (DCDC) converter failures during power cycles to reset stuck token bit managers (TBM) - necessitated a thorough refurbishment of the detector during Long Shutdown 2. The innermost layer of the barrel section was replaced, incorporating new versions of the PROC600 readout chip, TBM, and high density interconnect. New FEAST 2.3 DCDC converters were installed in the full detector, and damaged modules were replaced where accessible. The refurbished pixel detector was reinstalled in CMS in June 2021. A period of thorough commissioning followed, including the acquisition of 3.5 M cosmics tracks for alignment. This talk will summarize the refurbishment and commissioning of the pixel detector, as well as recent performance results from Run 3 operation.

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1. Introduction

The pixel detector [1] is the innermost component of the silicon tracking system of CMS [2] and provides four-hit coverage within $|\eta| < 3$. The barrel pixels (BPix) are made of four cylindrical layers that wrap around the beampipe at radii of 29, 68, 109, and 160 mm. The forward pixels (FPix) are made of three disks on each end of CMS, located between 309 and 508 mm in the longitudinal z coordinate from the interaction point. Each disk has an inner ring beginning at a radius of 45 mm and an outer ring beginning at a radius of 96 mm. The Phase-I pixel detector was installed in the winter of 2016 and 2017. The detector geometry is shown in Fig. 1.

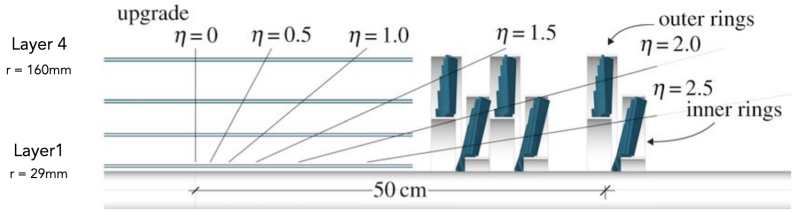

Figure 1: A view of the layout of a quarter of the pixel detector showing the four layers of BPix and three disks of FPix.

The detector is built from modules. Each module contains 66 560 n^+-in-n silicon pixels that are 100 μm by 150 μm with 280 μm active thickness, 16 readout chips (ROCs), a high density interconnect (HDI), and a base strip [3]. Each module has a token bit manager chip (TBM) glued and wirebonded to the HDI. BPix Layer 1 exceptionally has 2 TBMs per module to cope with higher hit rates. The different components of a pixel module are depicted in Fig. 2. There are 1 184 modules in BPix and 672 modules in FPix.

The ROCs have digital readout and double column draining. The ROCs used in BPix Layer 1, PROC600, are able to cope with hit rates up to 600 MHz/cm^2 and have dynamic cluster draining. The TBM receives the configuration data, clock, CMS L1 Trigger Accept (L1A) signal, and fast reset commands. It also orchestrates the readout of data from the ROCs once an L1A is received.

The detector has microTCA backend electronics, an open standard using Advanced Mezzanine Cards connected to a backplane, for control and data acquisition. Front-End Drivers (FED) control the readout and transmission of data to the CMS central data acquisition system. FEDs can only receive signals from the detector. Pixel Front-End Controllers (FEC) send configuration information to the ROCs and TBMs and distribute the clock and trigger via the Tracker Phase Locked Loop chip (TPLL). The clock additionally passes through a Quartz Phase Locked Loop chip (QPLL) to reduce jitter before reaching the TBMs.

Tracker FECs program registers on the electronics on the service cylinder and control the DCDC converters used in powering. Both types of FECs can send and receive information to and from the detector[4]. The DCDC converters receive an input voltage of 10 V and supply the analog (2.4 V) and digital voltages (3.3-3.5 V) to the TBMs and ROCs.

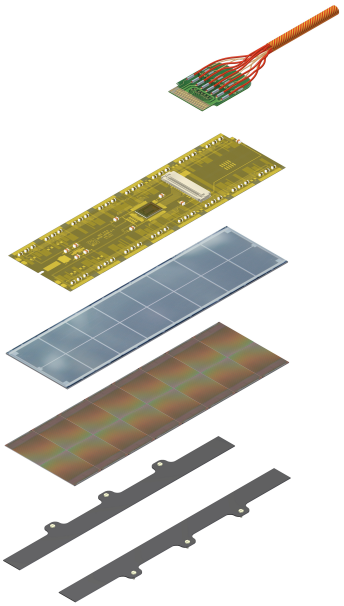

Figure 2: An exploded view of a pixel module with power and signal cables, HDI including TBM, silicon sensors, ROCs, and base strip.

2. Preparation and Performance in Run 3

The pixel detector was extracted at the beginning of Long Shutdown 2 and then kept cold and dry in a clean room to prevent reverse annealing. It was refurbished in preparation for Run 3. New DCDC converters robust against radiation damage were installed in the entire detector, and the pipes used for evaporative CO_2 cooling were reinforced for FPix. BPix Layer 1 was completely replaced with new modules. Besides being free of any radiation damage, the new Layer 1 has several improvements. The new version of the TBM has an additional delay setting, allowing Layers 1 and 2 to have different timing delays despite sharing a portcard. The ROCs have reduced dynamic inefficiency and crosstalk, and the HDIs were given a larger border that prevents high voltage shorts. A photo of an FPix half cylinder is shown in Fig. 3.

Throughout Run 3, the active detector fraction, hit efficiency, and cluster charge are monitored. Figure 4 shows the active detector fraction at the beginning of June 2023, with 98.4% of BPix and 97.9% of FPix used in data-taking. The hit efficiency is consistently high so far in Run 3, with the largest change seen in Layer 1, as shown in Fig. 5. The hit efficiency is affected by radiation damange, changes of bias voltage, updated settings obtained through gain calibrations, and annealing during time without beam. The resolution for hits in the pixel detector for 2022 and 2023 is listed in Table 1. The resolution has slightly degraded, which is expected for an aging detector.

Bias voltage scans are taken weekly during proton-proton collisions to check the optimal settings. The cluster charge is measured as a function of bias voltage, and the settings are updated accordingly. The cluster charge distributions are shown in Fig. 6. BPix Layer 1 receives the most radiation and its depletion voltage setting changes rapidly, as shown in Fig. 7.

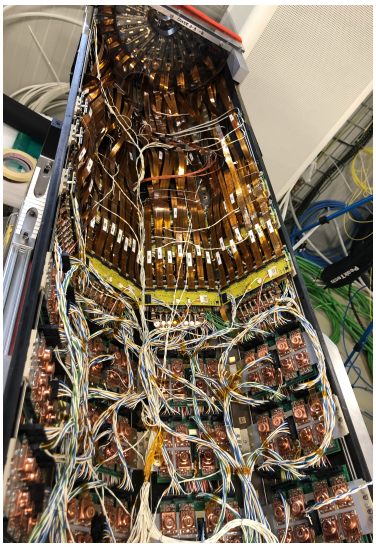

Figure 3: A half cylinder of FPix in the clean room during refurbishment and commissioning. The modules are visible at the top of the photo, and the DCDC converters are seen at the bottom of the photo.

Table 1: Comparison of hit resolution between years for BPix Layer 3 and FPix Disk 2. The resolutions are calculated by reconstructing a track using 3 hits and extrapolating the hit on the layer or disk of interest. The residuals with the actual hit are then calculated[5].

	2022	2023
BPix Layer 3 r-ϕ direction σ_r	9.80±0.12μm	11.03±0.11μm
BPix Layer 3 z direction σ_r	22.49±0.29μm	24.3±0.26μm
FPix Disk 2 r-ϕ direction σ_r	10.77±0.18μm	11.93±0.16μm
FPix Disk 2 z direction σ_r	18.39±0.33μm	21.01±0.29μm

3. Challenges during operations

During data-taking, if a channel fails to reliably transmit data, its readout will be stopped through a procedure called automasking. A channel in Layer 1 corresponds to 2 ROCs, a channel in Layer 2 corresponds to 4 ROCs, and a channel in Layers 3 and 4 and FPix corresponds to 8 ROCs. If a reconfiguration fails to recover the corresponding modules, they are blacklisted and will be DCDC powercycled at the next interfill. An anticipated and unavoidable cause of automasking occurs when a TBM is stuck as a result of an SEU. The BPix Layer 1 should be robust against this type of problem, yet it still had a relatively high number of automasked channels, as shown in Fig. 8. In this case, the channels were being automasked due to an unacceptably high number of out-of-sync errors from the FEDs. The high rate of automasking was diminished by adjusting a timing setting on the TBM which corresponds to the relative phase of the ROC and TBM and the phase of the 400 MHz data transmission. Once this adjustment was made, the level of automasking greatly reduced, as seen in the right plot of Fig. 8.

The detector had HV, LV, and control power turned off for a Technical Stop of the LHC in June 2023. When turned back on, a QPLL failed to lock to the LHC clock and has not been recovered.

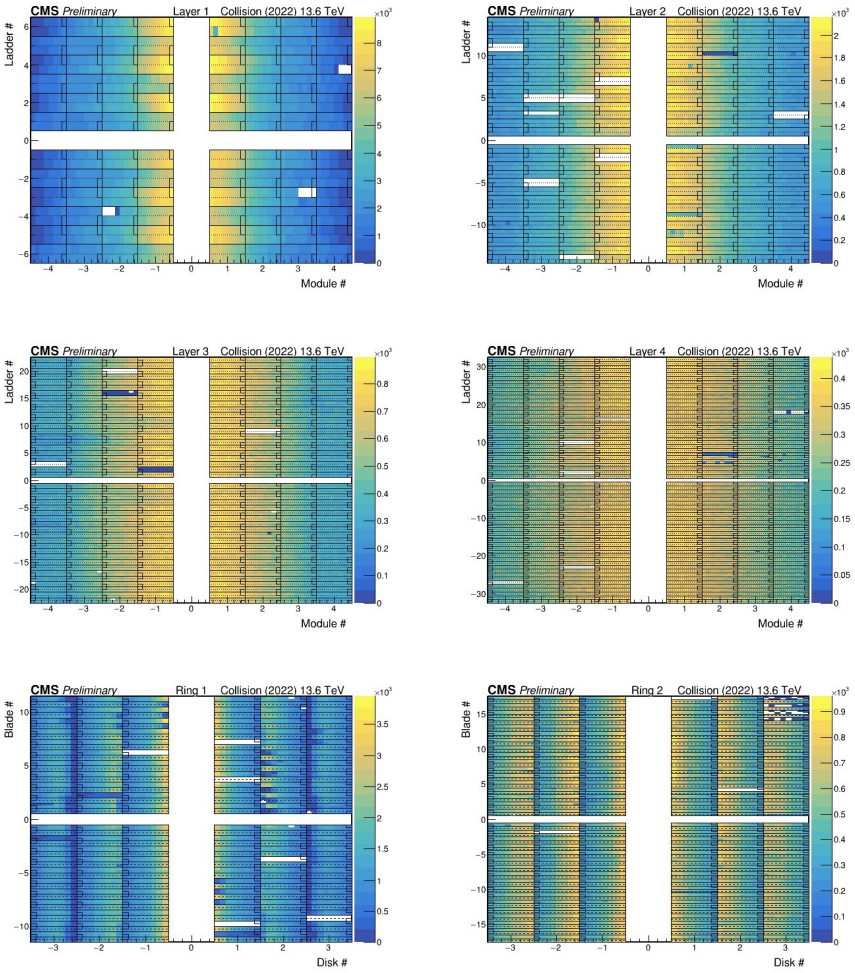

Figure 4: Occupancy plots of BPix Layer 1 (top left), Layer 2 (top right), Layer 3 (middle left), Layer 4 (middle right), FPix Ring 1 (bottom left), Ring 2 (bottom right).

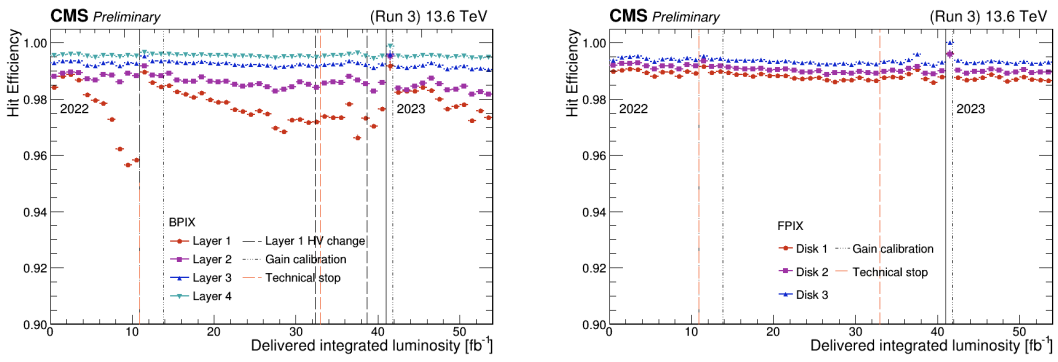

Figure 5: Hit efficiencies of different BPix layers and FPix rings over Run 3. The dip in BPix Layer 1 hit efficiency and subsequent recovery is a result of the bias voltage being adjusted[5].

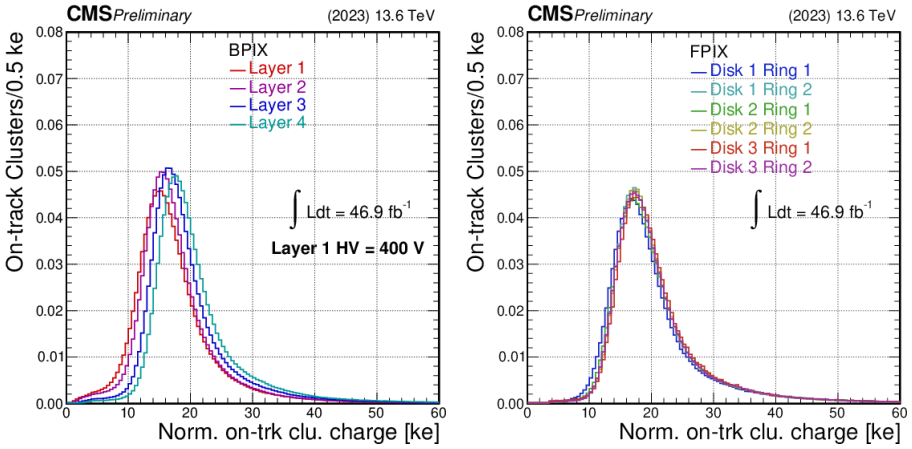

Figure 6: Cluster charge distributions of different BPix layers and FPix rings[5].

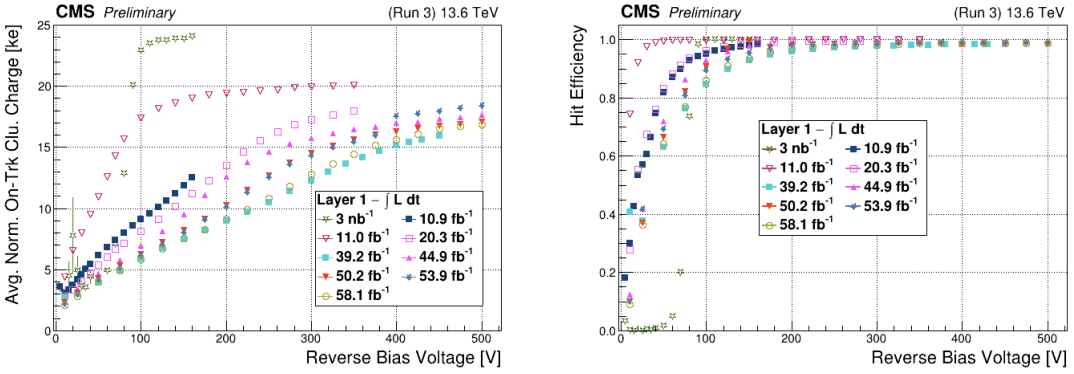

Figure 7: The cluster charge (left) and hit efficiency (right) of BPix Layer as a function of bias voltage. The different curves correspond to scans performed at various times in Run 3, denoted by the amount luminosity[5].

This led to a loss of 27 modules in BPix Layers 3 and 4 in the same ϕ-region. Recovering these modules would require replacing electronics on the service cylinder. Due to the large effort and inherent risks of this operation, a repair is not considered at this moment.

4. Summary and Outlook

The pixel detector performed reliably for the first years of Run 3, including during the heavy ion collision period at the end of 2023. The effects of radiation damage are observed through evolving performance in terms of efficiency, cluster charge, and other cluster properties. Bias voltage scans are performed regularly to ensure optimal settings are chosen for data-taking, especially in the case of BPix Layer 1. The level of automasked channels is now well under control with proper TBM settings, but the failure of one QPLL led to the loss of two tracking points in part of the detector.

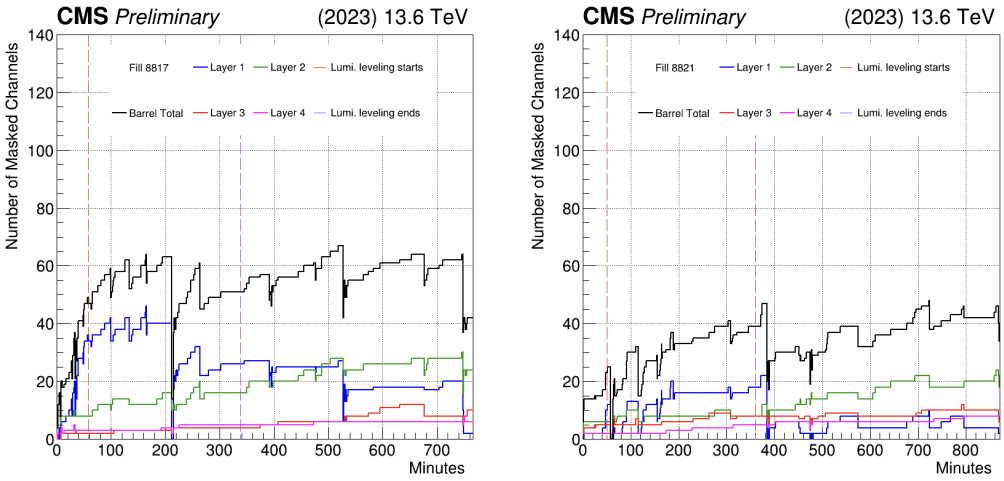

Figure 8: A comparison of the number of automasked channels between Fill 8817 (left) and Fill 8821 (right). The fills have comparable conditions: Fill 8817 had a peak luminosity of 2.05×10^{34} cm^{-2} s^{-1} and a peak pileup of 62.3, and Fill 8821 had a peak luminosity of 2.12×10^{34} cm^{-2}s^{-1} and a peak pileup of 64.3. Adjusting the 400 MHz data transmission phase greatly reduced the number of automasked channels in BPix Layer 1 [6].

References

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[3] CMS Collaboration, *CMS Technical Design Report for the Pixel Detector Upgrade*, CERN-LHCC-2012-016, CMS-TDR-011 (2012).

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[5] CMS Collaboration, *Pixel Detector Performance in early 2023*, (2023), URL:http://cds.cern.ch/record/2865842.

[6] CMS Collaboration, *Pixel Auto-masked Channels*, CERN-CMS-DP-2023-080,(2023), URL:https://cds.cern.ch/record/2876547.