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Operational experience of the Upstream Tracker of LHCb

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The LHCb experiment has faced a major upgrade in order to take data during Run 3 of the LHC with an instantaneous luminosity five times larger with respect to the previous runs. The Upstream Tracker (UT) is the new silicon strip tracking subdetector placed upstream of the LHCb magnet. It is fundamental to the particle reconstruction and plays an important role in the new software trigger. The installation of the UT has been completed in March 2023, representing a milestone for the experiment, and its commissioning phase is ongoing. This paper provides an overview of the status of the detector and details the ongoing work aimed at optimizing its functionality for the physics data acquisition.

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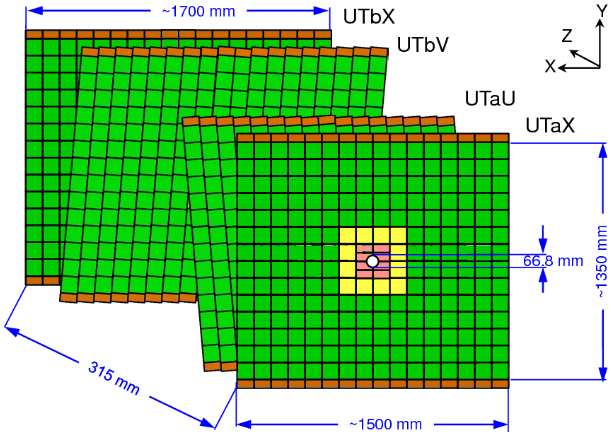

Figure 1: Layout of the Upstream Tracker of LHCb for Run 3 [1].

1. Introduction

The LHCb experiment is one of the four experiments situated along the Large Hadron Collider at CERN [1]. The main goal is to search for new physics by studying CP-violation and heavy flavour hadrons decays. New research topics have been added to its original goals, like heavy ion studies, exotic searches, and electroweak and fixed target physics. For this reason it can be considered a general purpose detector and its peculiar geometry has been designed to match its physics aims, which involve the study of particles with b and c quarks, particularly those sensitive to CP-violations. LHCb has taken data during the LHC Run 1 from 2010 to 2012 and the Run 2 from 2015 to 2018, collecting a total of 9 fb^{-1} of proton-proton (pp) data, about 30 nb^{-1} of lead-lead and p-lead collisions and about 200 nb^{-1} of fixed target data.

To enhance the precision of the physics results, it became necessary to accumulate a more extensive dataset. Consequently, the instantaneous luminosity has been increased by a factor of five during the Run 3, which started in 2022 and is ongoing, expecting a total luminosity of 50 fb^{-1} by the conclusion of Run 4. The previous Run 1-2 detector posed limitations on statistical improvements due to the presence of a hardware trigger, which would have been poorly efficient at higher luminosity. Addressing the challenge of $\mathcal{L} = 2 \times 10^{33}$ cm^{-2} s^{-1} necessitated a substantial upgrade of the detector. This involved the implementation of a fully software trigger operating at the LHC crossing rate of 40 MHz. To accommodate this change, all readout electronics were replaced, a new data acquisition system was developed, and nearly all the subdetectors were upgraded.

LHCb is a single-arm forward spectrometer covering a pseudorapidity range between 2 and 5. It is composed of a tracking system, made of the pixel silicon Vertex Locator (VELO), a silicon strip Upstream Tracker (UT) placed before the magnetic field, schematically pictured in Figure 1, and a Scintillating Fiber tracker (SciFi) downstream of the magnet. These tracking stations, combined with the magnetic field of 4 Tm, allow particle's trajectory reconstruction. To discriminate between different particles, a Particle Identification system is also present. Two ring imaging Cherenkov detectors (RICH1 and RICH2), one electromagnetic and one hadronic calorimeter and four stations for muon chambers.

2. The Upstream Tracker

The Upstream Tracker [2] is a new silicon strip subdetector of the LHCb experiment which plays a crucial role in the software trigger. Mainly it helps by reducing the ghost rate by a factor of two. It is important to improve the momentum resolution of the reconstructed charged particles, combining its hits with the tracks reconstructed in the VELO. It is also fundamental to reconstruct particles which decay after the VELO, such as long-lived particles.

The UT is composed of four layers, each one divided into two halves which close around the beampipe, the so called A-side and C-side. The silicon sensors are arranged on carbon fiber structures called staves, with dimensions of 99.5 mm x 1640 mm. In the first and last layers the staves and therefore the strips are vertically oriented, while in the central layers they are tilted by +/- 5 deg, in order to increase the resolution on the vertical component. Each stave has modules on both sides, alternating the modules and the readout electronics. The stereo layers host 16 staves each, while the other layers have 18 staves. The staves are enclosed in a box in order to keep them thermally insulated and protected from light and air. To prevent condensation, a dry gas is used. A CO_2 cooling system connects to the box and cools down the electronics with an S-shaped titanium cooling pipe running inside the staves.

The UT modules are composed of the silicon sensors and the front end readout electronics, glued and bonded to dataflex cables [3]. The silicon micro strip sensors have been developed in 4 different types, employed depending on their position in the layer to cope with different occupancies. The A-type have a p-in-n technology to be used in the outer region of the detector, with 512 strips with 187.5 μm pitch; the hybrids host 4 ASICs. All the other types use the n-in-p technology since they are displaced around the beam pipe, with 1024 strips and a pitch of 93.5 μm. The type C and D have a length which is half that of the other types. The D-type have a circular cut-out to conform to the beampipe. The front end ASIC is the Silicon ASIC for LHCb Tracking (SALT), it is a CMOS 130 nm technology, with 128 channels per ASIC. The SALT incorporates an analog processor along with a low-power (less than 1 mW/channel), high-speed (40 MSps) 6-bit ADC per channel. This is followed by a digital signal processor (DSP) block, a data formatting block and a serializer block. The DSP performs a pedestal subtraction, a mean common mode subtraction and a zero suppression. The ASIC is controlled via two different interfaces. One is the TFC which delivers the 40 MHz clock and other commands synchronised with the experiment clock, and the second one is the ECS which configures and monitors the ASIC through an I2C interface. The specifications of the SALT are in Table 1.

3. UT commissioning

The Upstream Tracker (UT) installation in the LHCb cavern was successfully completed in March 2023, marking the beginning of the data acquisition for the year. Subsequently, the UT underwent a commissioning phase to ensure its readiness for meaningful data collection. This commissioning process can be divided into three distinct categories: guarantee the detector's safety, optimize the data readout procedures, and ensure high data quality. The success of this process is imperative for the UT to fulfill its role and effectively collect physics data.

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In order to keep the detector safe and working in the nominal conditions a system of alarms has been developed. The conditions monitored are the humidity inside the box, the temperature of the staves and of the electronics, current and voltage. For these, monitoring panels have been developed and the alarms are linked to sensors in the detector. Additionally, a Detector Control System is in place to take action when the set range is exceeded. The temperature is maintained at the nominal value by a cooling system which uses CO_2 for the modules and water for the peripheral electronics.

Once the well-being of the UT is ensured, data has to be extracted. For this reason firmware has been implemented which transforms the data from ASIC to PCIe format via PCIe40 cards hosting arrays of optical transmitters and receivers connected to a powerful Intel Arria 10 FPGA [1]. The firmware has been developed in five different flavours to cope with different occupancy in the detector, reading a different number of ASICs and e-links depending on the position in the layer. It can work both in zero-suppressed and non-zero-suppressed mode. The Experiment Control System has been developed to control and configure the back-end and front-end electronics; in addition it is a powerful debugging tool during the commissioning.

Finally it is important to develop tools to check the data quality. Many datasets have been collected in the early stage of the commissioning in bypass mode, mainly without the serialization of the Tell40, for the characterization of the hybrids to illustrate the behaviour of the detector. The same tests have been performed before and after the installation in the cavern and good agreement of noise and bad channels has been found. To get the noise values, the pedestal is computed as the constant offset for each read-out channel. The Mean Common Mode (MCM) noise is the fluctuation in time of the signal baseline, which is computed as an average noise over channels without signal. Finally we subtract the MCM noise and the pedestal from the ADC raw values and the root mean square is computed to finally get the noise. The values of the noise and pedestals have been monitored over time and found to be constant. About 0.16% of the channels are classified as bad channels, mainly by observing a pedestal shift or high noise values. In order to automate these checks of the noise and pedestals, dedicated software called VETRA has been implemented and merged in the LHCb official software. In addition to the offline analysis, VETRA's goal is to perform an automated calibration: pedestals and the thresholds to run in zero suppression mode can be computed using the End of Fill data, meaning non-zero suppressed data without the LHC beam. Through the ECS these parameters are updated in the detector in order to take zero suppressed data with precise knowledge of the noise. A fundamental tool to check the data quality is the monitoring. It takes a small sample of the captured data and sends it to the computer farm to monitor in real time basic information, such as the hits per sensor, errors information and analogue response. Finally a time alignment has been performed with the data collected during the 2023 LHC Ion Run. This step is crucial to ensure synchronisation of the experiment with the LHC clock.

4. Conclusions

The Upstream Tracker is part of the LHCb Experiment's tracking system. It has been installed successfully and is undergoing commissioning. The first commissioning data have been collected and analysed. The performance studies show a match with the specifications. During the 2023 end of year technical stop, the goal is to recover 99% of the detector efficiency, with adjustments of

Table 1: SALT ASIC specification.

Variable	**Specification**
Input / Output pitch	80 µm / 140 µm
Total power dissipation	$<$ 768 mW
Radiation hardness	0.3 MGy
Sensor input capacitance	1.6–12 pF
Noise	$\approx 1000\,e^-$ @10 pF + 50 e^-/pF
Maximum cross-talk	Less than 5% between channels
Signal polarity	Both electron and hole collection
Dynamic range	Input charge up to 30,000 e^-
Linearity	Within 5% over dynamic range
Pulse shape and tail	$T_{peak} \approx 25$ ns, amplitude after $2\times T_{peak} < 5\%$ of peak
Gain uniformity	Uniformity across channels within $\approx$5%
ADC bits	6 bits (5 bits for each polarity)
ADC sampling rate	40 MHz
DSP functions	Pedestal and MCM subtraction, zero suppression
Output formats	Non-zero suppressed, zero suppressed
Calibration modes	Analogue test pulses, digital data loading
Output serialiser	Three to five serial e-links, at 320 Mbit/s
Slow controls interface	I2C
Fast digital signals interface	Differential, SLVS

the electronics and with mechanical interventions. The stability of the datataking is one goal to be reached for 2024, in which the UT will run in global LHCb datataking.

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