PROCEEDINGS OF SCIENCE

Ideas for further upgrades of the CMS Inner Tracker

Duccio Abbaneo[a,*] on behalf of the CMS collaboration

[a] *CERN, Esplanade des particules 1, CH-1211, Geneva, Switzerland*

E-mail: Duccio.Abbaneo@cern.ch

The High Luminosity Large Hadron Collider (HL-LHC) at CERN is projected to provide an integrated luminosity of up to 4000 fb^{-1} over its operational span, extending beyond 2040.The CMS Phase-2 Inner Tracker, scheduled for installation at the end of Long Shutdown 3, has been designed to meet the demands of the high-luminosity operation. However, despite a careful optimisation for radiation tolerance, the projected lifespan of silicon sensors and electronic components indicates that the modules in the inner regions and some of the auxiliary electronics will not be able to function correctly for the entire duration of the HL-LHC program. Consequently, those components will need to be replaced at least once during the operation.

Currently, more advanced technologies are under development for readout ASICs and data links, for applications in future High-Energy Physics (HEP) detectors. These technologies may offer opportunities to further enhance the performance of the CMS Inner Tracker for the latter half of the HL-LHC program. Two lines of research are being explored: (i) the improvement of the inner regions, to achieve reduced material budget and enhanced tracking performance, and (ii) the implementation of precision timing in the very forward region to extend the coverage of timing information in CMS up to $\eta = 4$.

Some of the ideas under consideration are presented in this manuscript.

The 32nd International Workshop on Vertex Detectors (VERTEX2023)
16-20 October 2023
Sestri Levante, Genova, Italy

[*] Speaker

PoS(VERTEX2023)036

1. Introduction

The CMS experiment [1] at the CERN LHC will undergo a major upgrade for the High-Luminosity LHC (HL-LHC) phase [2]. The CMS Inner Tracker [3] (IT) is designed for maintenance accessibility during Long Shutdowns and Year-End Technical Stops of the LHC. It is composed of a four-layer barrel section (TBPX), eight small forward disks (TFPX), and two more end-caps with larger disks (TEPX). The layout of the IT is shown in Fig. 1. After approximately half of the planned HL-LHC operation, the modules in the innermost TBPX layer and TFPX ring, along with the electronics boards located on the outer surface of the TFPX, will need replacement to mitigate radiation damage degradation.

Developments such as the 28 nm CMOS ASIC technology and silicon photonics data links pave the way for enhancing detector performance in the latter half of the HL-LHC program. Concurrently, further upgrades of the IT offer concrete, medium-term applications for ongoing R&D activities.

Two key areas are under exploration: (i) enhancing the inner regions to improve tracking performance, and (ii) implementing precision timing in the TEPX disks, extending the timing information coverage of CMS up to $\eta = 4$.

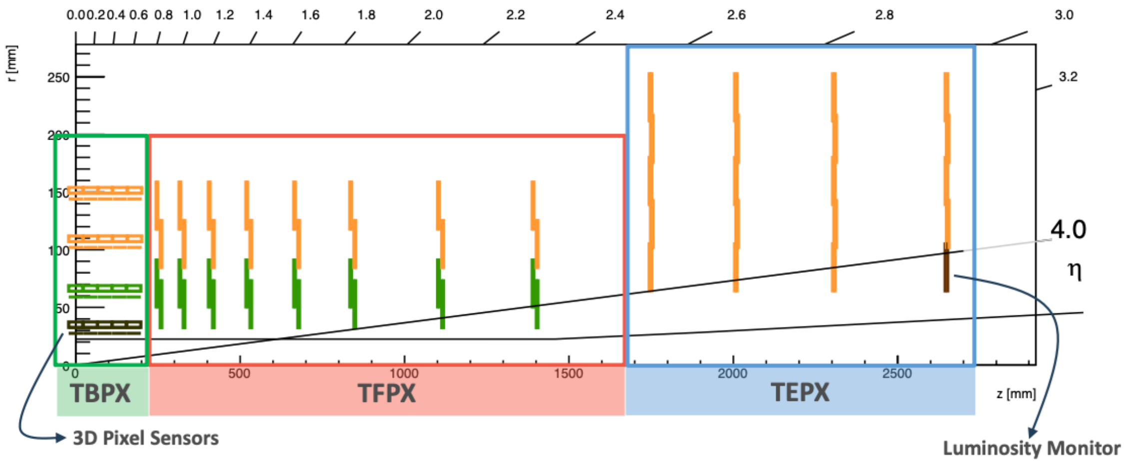

Figure 1: Layout of the CMS Phase-2 Inner Tracker under construction for the HL-LHC.

2. Improvement of the inner regions

The goal of enhancing the inner regions with advanced technologies is to improve tracking resolution near the interaction point. Enhanced resolution in transverse and longitudinal impact parameters, d_0 and z_0, leads to better b-tagging performance and improved pile-up mitigation, benefiting the overall physics program of CMS.

Three layouts were assessed:

"Small": Pixel size is reduced by 0.6 compared to the "standard" HL-LHC layout, from $25 \times 100\,\mu\text{m}^2$ to $15 \times 60\,\mu\text{m}^2$. Active sensor thickness and precision of charge measurement in the readout chip (Time Over Threshold) are similarly scaled, achieving a 0.6 factor improvement in hit resolution without altering occupancy and bandwidth. The change targets the first two layers of TBPX and the first two rings of TFPX.

"Standard light": Maintains the pixel size of the "standard" HL-LHC layout but reduces the mass of modules by 15%, applied in the same regions as "small".

"Small heavy": Combines the reduced pixel size of "small" with a 15% increase in module mass.

Figure 2 summarizes the findings for particles with transverse momentum greater than 0.9 GeV/c in minimum-bias events.

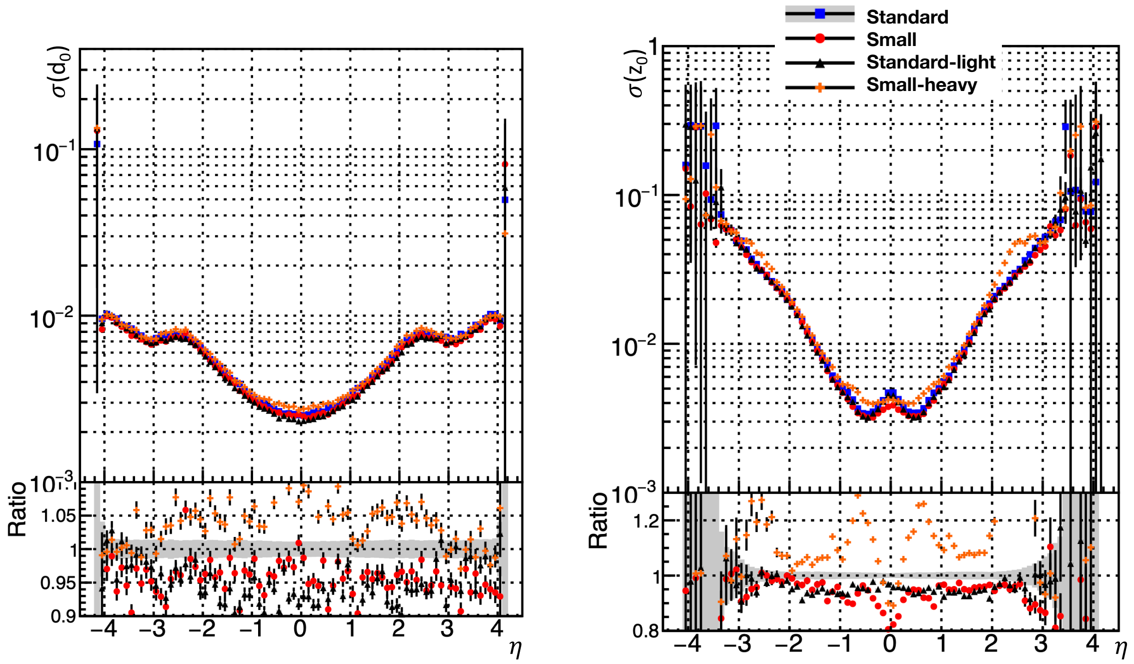

Figure 2: Comparison of d_0 and z_0 resolutions for "small", "standard light", and "small heavy" layouts against the "standard" HL-LHC layout.

The "small" layout shows an average improvement factor of about 0.95 in d_0 and z_0 resolutions compared to the "standard", despite the much more significant (factor of 0.6) hit resolution improvement. This indicates that multiple scattering heavily affects tracking resolution, diminishing the benefits of improved hit resolution.

"Standard light" shows similar or better tracking resolution improvements across most of the rapidity range compared to "small".

However, "small heavy" shows performance degradation compared to "standard" in most of the rapidity range.

These results suggest that reducing detector mass is as crucial, if not more, than enhancing hit precision. Smaller pixels offer limited benefits and can become counterproductive if the higher granularity implies an increase of the material budget, because of higher power density.

In the HL-LHC IT design, power density is a major determinant of material contributors like pipework size and cooling contact mass, as well as power distribution conductor cross-sections. Therefore, the following design guidelines emerge.

Design guidelines for the inner regions upgrade. Minimizing power budget is paramount for the inner region's upgrade. 3D sensors remain essential for TBPX layer 1, as planar sensors impose more demanding cooling requirements leading to increased mass. While maintaining HL-LHC detector granularity and functionality as a baseline, any enhancements must be weighed against power budget impacts. Among chip specifications, besides minimizing power budget, lowering the detection threshold is beneficial, as it helps maintaining good hit resolution as sensors lose charge collection efficiency due to radiation damage. Advanced technologies for readout chips and data links must be accompanied by an aggressive low-mass system design to achieve a significant performance improvement.

3. Forward timing disks

Precision timing detectors, introduced in the HL-LHC upgrade of CMS [4], currently cover the rapidity range $|\eta| < 3$. Integrating timing information aids pile-up mitigation, crucial for maintaining or enhancing the physics reconstruction performance of CMS in high-luminosity conditions.

Extending timing coverage to $|\eta| < 4$ is achievable by adding timing information to one or two TEPX disks. Figure 3 illustrates this benefit in a study where two Higgs bosons from Vector Boson Fusion decay into four b quarks. In this study a timing precision of about 30 ps was assumed for reconstructed tracks up to $|\eta| < 4$, which could be realized with two timing disks and a per-coordinate precision of about 50 ps. The inclusion of timing information reduces pile-up jet background by about a factor of two, without significant loss of signal b and VBF jet efficiency.

Implementing timing in TEPX disks could be realized using small-pitch LGAD sensors, combining spatial and timing precision. At the high-rapidity edge, sensors face a fluence of approximately $3 - 4 \times 10^{15}$ 1 MeV n_{eq}, decreasing by about a factor of four across the disk. This is challenging for LGAD sensors, but possibly achievable with design optimization.

Two options are being considered.

Trench-Isolated LGAD sensors [5] seem to be a suitable option to provide the required performance. In such sensors, by design, the signal from a traversing particle is almost always contained in a single pixel, hence the position resolution is binary. In order to maintain the tracking precision of the HL-LHC detector, a pixel size of $50 \times 50\,\mu\text{m}^2$ would be required[1]. The combination of high granularity with precision timing is demanding for the readout ASIC development, possibly requiring a high power budget.

Alternatively, an R&D on DC-coupled resistive LGAD sensors, also known as Resistive Silicon Detectors (DC-RSD) [6] , is ongoing with the goal of developing sensors capable of charge sharing over a limited area of 2×2 cells. With such sensors, the hit resolution would be significantly better than the binary resolution, potentially reaching up to $1/10$ of the pixel size. Hence larger pixels could be implemented, maintaining the tracking precision of the HL-LHC detector and at the same time moderating the power budget. A cell size of $100 \times 100\,\mu\text{m}^2$ is considered as working hypothesis, since with charge contained in 2×2 cells such granularity would suit the hit occupancy of TEPX disks, keeping the hit-merging probability at an adequate level. It seems plausible that

[1]While the rectangular aspect ratio is necessary in the barrel, which led to the implementation of $25 \times 100\,\mu\text{m}^2$ pixels in the HL-LHC detector, square or rectangular pixels yield equivalent performance in the TFPX and TEPX disks.

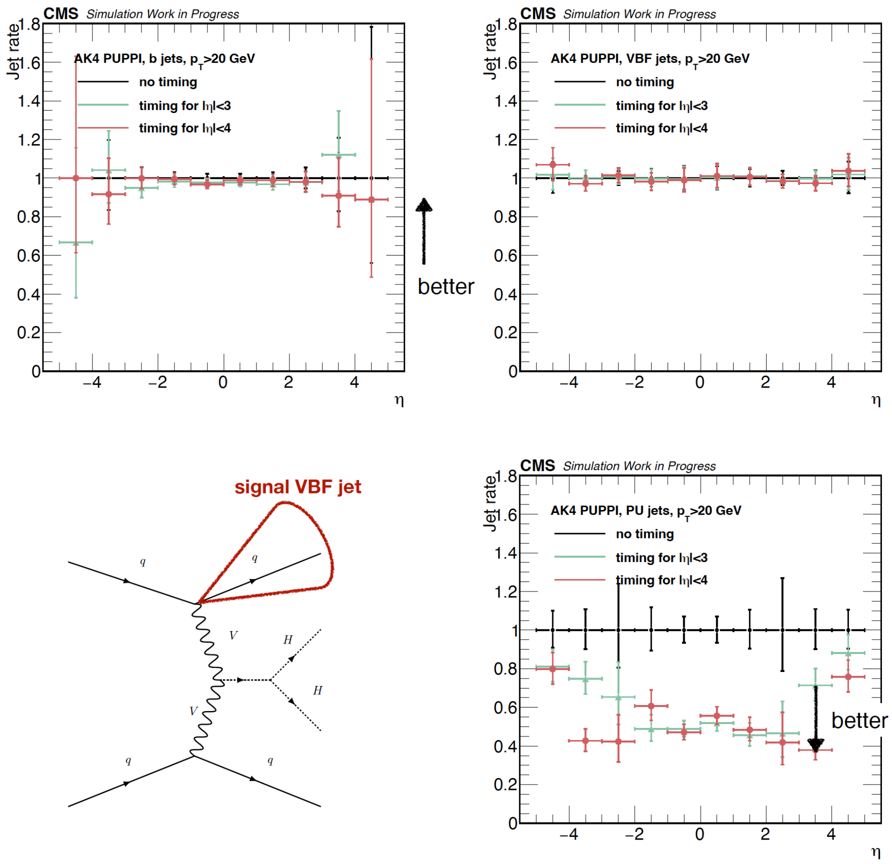

Figure 3: Ratio of selection efficiencies with and without timing information for signal b and VBF jets as well as background pile-up jets, in a channel with two-Higgs bosons from VBF decaying to four b quarks.

with a reduction in granularity by a factor of 4 compared to the inner regions, the readout chip could be realized within a comparable power budget, despite the introduction of precision timing.

4. Conclusions and outlook

Based on the arguments discussed above, the following basic requirements can be listed for the readout chips of the inner regions and the timing disks, assuming the use of DC-RSD in the timing disks. The development can be structured as a single chip with two front-end variants, sharing overall architecture and periphery.

Inner regions	**Timing disks**
Pixel size $25 \times 100\,\mu\text{m}^2$	Pixel size $100 \times 100\,\mu\text{m}^2$
Detection threshold $\ll 900\,\text{e}^-$	Timing resolution $< 50\,\text{ps}$
Power density $\ll 0.6\,\text{W/cm}^2$	Power density $\leq 0.6\,\text{W/cm}^2$

Chip size (h × w) $16.8 \times 21.6\,\text{mm}^2$
Output bandwidth $\leq 5\,\text{Gbps}$
Serial powering infrastructure
Trigger and latency as in the HL-LHC detector
Interface to silicon photonics link

Enhancing the performance of the inner regions significantly also entails an aggressive, low-mass system design for the TBPX stave. Innovative solutions and optimal assembly techniques, akin to those used in the ALICE ITS stave [7], need to be developed.

The key elements would be the development of a lightweight carbon space frame with embedded pipework compliant with high-pressure CO_2 cooling operation: that could be achieved starting from the ALICE structure construction, replacing polyimide pipes with titanium (Fig. 4 left). Single sensor-chip assemblies could be mounted directly on the support structure, and coupled to an integrated flex circuit for power and readout, wire-bonded to the periphery of the chips. The flex would be carrying an end-of-stave data concentrator and photonics chip (Fig. 4 right), with one optical link per stave. Such stave concept has the potential of a significant mass saving compared to the current HL-LHC design.

Significant advancements in sensor R&D and 28 nm CMOS chip developments are expected in 2024, potentially enabling an upgrade proposal with consolidated specifications by year-end.

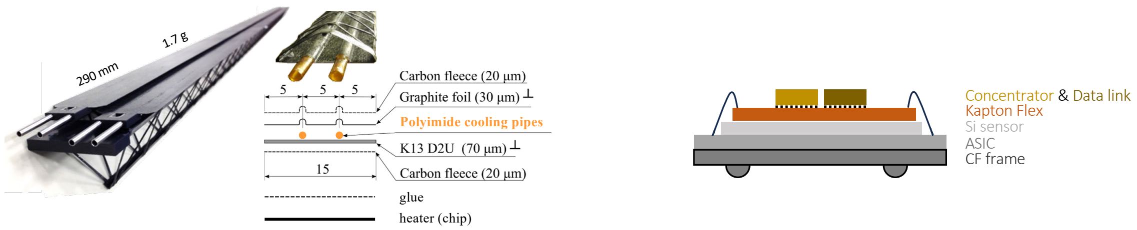

Figure 4: Left: mechanical structure of the ALICE ITS stave. Polyimide pipes could be replaced with titanium pipes, to comply with high-pressure CO_2 operation. Right: cross sectional view of a possible future TBPX stave concept.

References

[1] The CMS Collaboration, The CMS Experiment at the CERN LHC, JINST 3 (2008), http://dx.doi.org/10.1088/1748-0221/3/08/S08004

[2] I. Zurbano Fernandez, et al., High-Luminosity Large Hadron Collider (HL-LHC): Technical design report, CERN-2020-010, https://doi.org/10.23731/CYRM-2020-0010

[3] The CMS Collaboration, The Phase-2 Upgrade of the CMS Tracker. CERN-LHCC-2017-009, https://cds.cern.ch/record/2272264

[4] The CMS Collaboration, A MIP Timing Detector for the CMS Phase-2 Upgrade. CERN-LHCC-2019-003, https://cds.cern.ch/record/2667167

[5] M. Senger at al., A Comprehensive Characterization of the TI-LGAD Technology, Sensors 2023, 23, 6225, https://doi.org/10.3390/s23136225

[6] L. Menzio et al., DC-coupled resistive silicon detectors for 4D tracking. Nucl. Instrum. Meth. Phys. Res. A 2022, 1041, https://doi.org/10.1016/j.nima.2022.167374

[7] The ALICE Collaboration, Technical Design Report for the Upgrade of the ALICE Inner Tracking System. CERN-LHCC-2013-024, https://cds.cern.ch/record/1625842