PROCEEDINGS OF SCIENCE

The DMAPS Upgrade of the Belle II Vertex Detector

D. Xu[a,*], M. Babeluk[b], M. Barbero[a], J. Baudot[c], T. Bergauer[b], F. Bernlochner[h], G. Bertolone[c],S. Bettarini[d,e], F. Bosi[d,e], R. Boudagga[a], P. Breugnon[a], Y. Buch[j], G. Casarosa[d,e], J. Dingfelderd[h] , G. Dujany[c], L. Federici[c], T. Fillinger[b], C. Finck[c], D. Fougeron[a], F. Forti[d,e], A. Frey[j], A. Himmi[c], C.Hu[c], C. Irmler[b], M. Karagounis[h], A. Kumar[c], C. Marinas[f], M. Massa[d], L. Massaccesi[d,e], J. Mazzora de Cos[f], M. Minuti[d,e], S. Mondal[d,e], K.R.Nakamura[g], H. Pham[c], P. Pangaud[a], I. Ripp-Baudot[c], G. Rizzo[d,e], C. Schwanda[b], B. Schwenker[j], P. Stavroulakis[c], I. Valin[c], C. Wesseland[h,i] on behalf of the Belle II VTX upgrade group.

[a] *Aix Marseille Université, CNRS/IN2P3, CPPM,*
13009 Marseille, FranceInstitution,

[b] *Institute of High Energy Physics(HEPHY), Austrian Academy of Sciences*
1050, Vienna, Austria

[c] *Université de Strasbourg, CNRS, IPHC, UMR7178,*
F-67000 Strasbourg, France

[d] *INFN Sezione di Pisa,*
I-56127, Pisa, Italy

[e] *Dipartimento di Fisica, Università di Pisa,*
I-56127, Pisa, Italy

[f] *Instituto de Fisica Corpuscular(IFIC),CSIC-UV,*
Paterna 46980, Spain

[g] *High Energy Accelerator Research Organization (KEK), Tsukuba,*
305-0801, Japan

[h] *University of Bonn,*
Nussallee 12, 53115 Bonn, Germany

[i] *Deutsches Elektronen-Synchrotron*
22607 Hamburg, Germany

[j] *Georg-August Universität,*
Freidrich-HundPlatz 1 Göttingen, German

[*] Speaker

PoS(VERTEX2023)041

E-mail: xudanwei@cppm.in2p3.fr

Abstract: In order to profit from the increased luminosity provided by the SuperKEKB accelerator in the future, improvements should be brought to the current Belle II detector. The Belle II collaboration has thus proposed the upgrade of the current inner vertex detector to a new VTX vertex detector, with the target to cope with a higher luminosity. A new DMAPS sensor named OBELIX is proposed and is expected to be submitted in 2024. The design of the OBELIX ASIC is based on a previously designed prototype TJ-Monopix2 chip, and will feature a completely new digital periphery.

The 32nd International Workshop on Vertex Detectors (VERTEX2023)
16-20 October 2023
Sestri Levante, Genova, Italy

1. Requirements for the Belle II Upgrade

The Belle II detector operates since 2019 at the SuperKEKB collider, the asymmetric energy e+e- Super B-Factory in Tsukuba, Japan. Belle II [1] is an experiment designed to make precise measurements of weak interaction parameters and find New Physics beyond the Standard Model of particle physics. In June 2022, SuperKEKB achieved a new luminosity world record of $4.7\times10^{34}cm^{-2}s^{-1}$, but there is still a gap by one order of magnitude from its target luminosity ($6\times10^{35}cm^{-2}s^{-1}$). It should be noted that the future beam background is very dependent on the evolution of machine related parameters. In order to cope with the higher luminosity which is anticipated to be provided in the future by the accelerator, an upgrade of the current vertex detector named VTX is proposed. The requirements for the Belle II VTX detector are listed in Table 1.

Table1. Belle II VTX requirements from simulations

Spatial resolution	< 10-15μm
Material buget (inner to outer) layers	0.1%X_0 for L1&L2, 0.4%X_0 for L3, 0.6%X_0 for L4, 0.8%X_0 for L5
Max hit rate	120MHZ/cm^2
Time precision	<100ns
Trigger freq&delay	30kHz & 5-10μs
Rad. Hard TID	<100 kGy/year
Rad. Hard fluence	~ $5\times10^{13}n_{eq}/cm^2$/year
Power consumption	<200 mW/cm^2

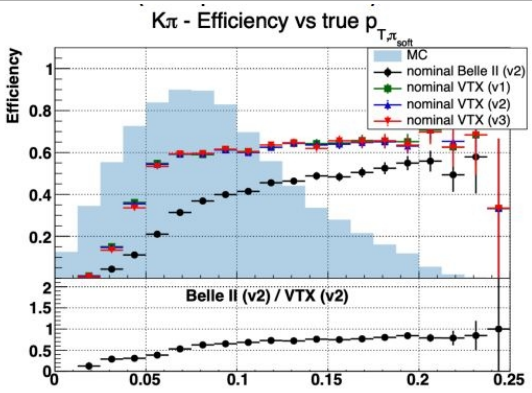

Figure 1: tracking performance comparison between the current VXD and the new VTX

This new silicon pixel detector tracker aims to be both more robust against the expected higher level of machine background and more performant in terms of precision and standalone track finding efficiency. Track performance simulations were performed and Figure 1 shows a sample of the results. In Figure 1, we can see that the VTX can provide a better tracking efficiency resolution than the current VXD at low momentum. The new VTX contains 5 active detection layers and in order to fit into the existing space, the innermost and outermost radii need to be within the range of 14 mm and 14 cm. All layers are planned to be equipped with a thin, radiation-hard and fully depleted monolithic active pixel sensor called OBELIX. In the following sections, the TJ-Monopix2 chip, from which OBELIX is derived, will first be

described. Selected test results will be given. Finally, a description of the changes brought to the OBELIX design will be shown.

2. A forrunner sensor: TJ-Monopix2

An initial work was done to identify which technology could fulfil the requirements of the VTX environment. TJ-Monopix2 is an ASIC that was developed for the specifications of the outermost layers of the ATLAS pixel detector, which has similarities to the specifications of the OBELIX ASIC in terms of the foreseen radiation level and time-stamping speed needed. The sections below describe TJ-Monopix2 and the tests performed to validate its usage in the VTX context.

2.1 Design

The TJ-Monopix2 is manufactured in TowerJazz 180nm CMOS imaging process. A low dose deep n implant is added under the pixel matrix to enhance radiation tolerance [2]. The front-end is derived from ALPIDE[3], and the readout is based on a column-drain architecture [4]. TJ-Monopix2 was submitted at the end of 2020 and came back from production at the beginning of 2021.

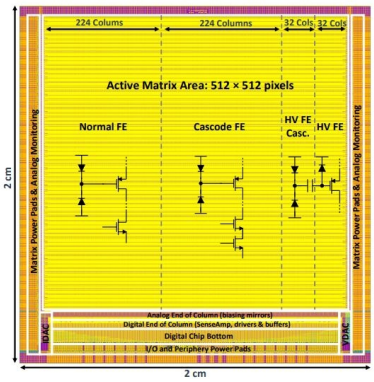

Figure 2: Layout of the TJ-Monopix2

The overall layout of the TJ-Monopix2 prototype is shown in Figure 2. The chip size is equal to 2×2cm^2 and the pixel size is 33.04×33.04μm^2 with the matrix consisting of 512×512 pixels split in four sectors with variations in front-end design made for testing purposes. The size of the BCID bus has been set to 7-bits which allows a maximum ToT of approximately 2 μs without affecting the in-time efficiency of the readout architecture [5]. To increase the front-end immunity to power supply noise, the discriminator and pre-amplifier grounds have been separated. The periphery is designed to simplify system integration by essentially requiring two sets of input signals (clock and data) for the communication uplink and downlink in order to operate the chip. The readout to the DAQ is achieved through a Low Voltage Differential Signaling interface (LVDS) with a speed up to 320 Mb/s [5].

2.2 Test Results

As TJ-Monopix2 is the basis on which the OBELIX design is built, many tests have been performed on the chip in our community that can be described in three categories:

- Full characterization on laboratory test bench: threshold and noise scans, calibrations
- Test-beam at DESY for detection efficiency and position resolution measurements
- NIEL irradiation campaigns to test radiation hardness

Characterization tests have been performed in several laboratories since the coming back of the chip from the factory and are still ongoing. As the lab test are described in depth in another proceeding [6], here we will mainly present the test-beam results. A total of two sessions of tests under beam has been conducted so far, the first in June 2022, and the later one in July 2023. In the first test, we set the detection threshold at 500 e$^-$ and we could measure a hit

detection efficiency above 99.5% for unirradiated samples, and a cluster position residual at around 9.15 micron.

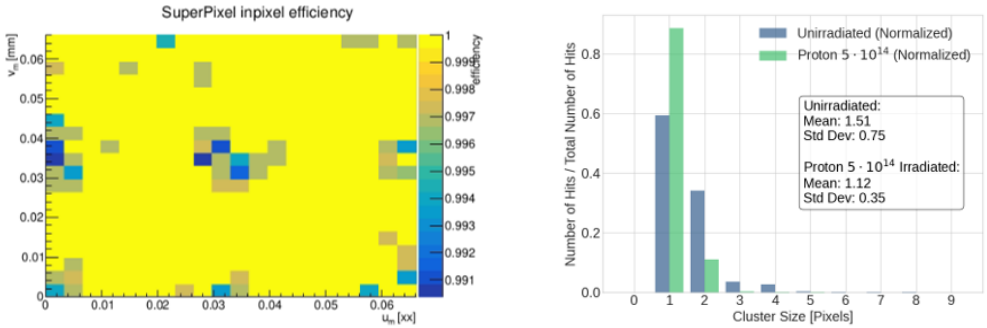

Figure 3,4: Test-beam results for TJ-Monopix2 (threshold at 310 e^- and with irradiated chip W05R16)

For the latest test beam results, the settings were improved and a detection threshold between 200 and 300 e^- could be set. Figures 3 and 4 above show the preliminary results from this second test-beam campaign. The super pixel efficiency, which scrutinizes the 2×2 pixel segment where each individual pixel within the entire matrix is projected, provides insights into the distribution of efficiency across pixels (see Figure 3). Notably, at the center of the pixels, the efficiency attains significantly higher levels compared to the peripheries or intersections, where a gradual decline is observed. Even within the less favorable regions of the pixel, the detection efficiency maintains a good level, consistently surpassing 98%. In Figure 4, a reduction in cluster size is observed after irradiation of the chip to $5\times10^{14}n_{eq}/cm^2$. Figure 5 further illustrates the cluster position residuals, which reach around 9.5 µm for this irradiated sensor. These are encouraging preliminary results of the ongoing test-beam analysis, which satisfy the need of the Belle II upgrade, and further in-depth analysis is on-going.

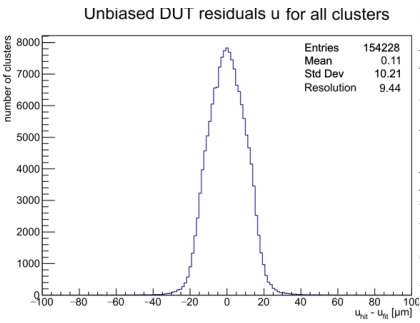

Figure 5 : Cluster position residual

3. The OBELIX design

As of the current time of writing, the OBELIX prototype in TowerJazz 180nm technology is in an advanced design state, yet it remains a work in progress. The OBELIX design has inherited the pixel matrix of TJ-Monopix2 but it almost doubles its area and introduces a novel digital periphery including a trigger logic. The adaptation is essential to align with the required time-stamping resolution and maximum hit rate stipulated by the Belle II VTX upgrade project. Additionally, a power regulator is incorporated for mitigating voltage drop on supply rail and to streamline system integration. The top floorplan of OBELIX design is shown in Figure 6.

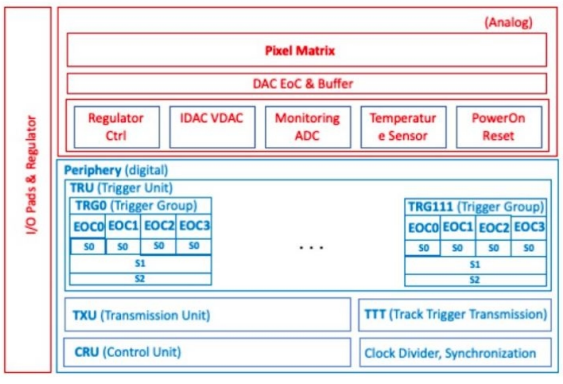

Figure 6 : OBELIX top floorplan

3.1 Analog design

For what concerns the analog part of OBELIX, the design of TJ-Monopix2 is basically transplanted driven by the conviction the TJ-Monopix2 design can cover most of the requirements of Belle II detector according to the test results. Nevertheless, the OBELIX matrix is bigger and will be made of 464 rows and 896 columns. The chip however has several additional features in its periphery, such as a 10-bit monitoring ADC, a power-on reset, temperature sensor and on-chip regulator. The choice of a specific front-end flavour from TJ-Monopix2 is a topic of ongoing discussion with several options still opened, since all front-end flavours have shown comparable performance. In addition, the power distribution is one crucial point of attention, as the OBELIX chip is larger than TJ-Monopix2 and the voltage drop could result in performance degradation. The strategy used in OBELIX is to power the matrix from both sides using the top metal level (Metal 6). At the bottom, the DAC_EOC (End-of-Column) buffer replicates the bias voltage of each double column (DC) and readjusts its bias current so that it remains unchanged from one DC to the other. Vertical power drop will be mitigated by the addition of LDOs on both sides of the matrix. Currently, the OBELIX fits in the power budget of 200 mW/cm^2 if we stick to 100 ns BCID precision and exceeds the power budget by 10% if we change for a BCID precision of 50 ns.

3.2 Digital design

According to the requirements, the digital periphery should support a maximum hit rate of 120 MHz/cm^2 and should handle a trigger rate of 30 kHz with a latency of 5 to 10 μs. Besides, the main input clock comes at 160 MHz and several clocks need to be derived for various domains. Since the clock needs to be aligned with the Belle II main RF clock, the real frequency will be 169.7 MHz. The readout will be made with a single output at a rate of 320 Mb/s.

The digital periphery is quite different from the periphery of TJ-Monopix2, mainly because of the addition of the new End-of-Column structure and the new trigger mechanism. Corresponding to the module concept and function distribution of the periphery, and combined with the new specifications of OBELIX, we have proposed a top digital circuit which is divided into four modules. The synchronization unit(SCU) is used for generating the divided clocks that the chip needs and to synchronize the data received at the input. The control unit (CRU) implements the RD53B command protocol and includes a register control. For the command decoder, we almost keep the design of TJ-Monopix2, but we modified several commands according to the requirements of others parts in the chip. The trigger unit (TRU) manages pixel data that come from the matrix and waits for the trigger command to pick them out for output. Finally, the transmission unit (TXU) generates the output data for external transmission. There are two new added design features in this chip. One is the PTD, periphery time to digital, which is a part of the TRU and is used for precision timing of the pixel hits. Since the timing resolution from BCID of 50 ns is not great, as it saves a lot of power compared to TJ-Monopix2, this feature can help to improving the timing by adding an internal counter that uses the fast 160 MHz clock. The other feature is the TTT, track trigger transmission, that could provide an alternative contribution to the Belle II trigger system. It can give a fast coarse information on hit position, and it has a separate transmission schema with respect to the general data output. Due to power consumption limitation, these two functions will only be available for the outer layers

of VTX. The overall digital design is almost finished, and it is currently at the stage of back-end process.

4. Conclusions

This paper describes the status of the OBELIX chip for the Belle II vertex detector upgrade VTX. Based on the latest TJ-Monopix2 pixel prototype, this novel CMOS pixel sensor is being developped. The meticulous characterization of the TJ-Monopix2 sensor matrix is decisive for the OBELIX design proposal and thus far, the lab test results have been quite positive. Sustained module operation over long times in a first test-beam and new test-beam results with irradiated sensors are still under analyses, but so far the preliminary results are quite positive. OBELIX will be used across all layers of the upgraded VTX vertex detector, but due to power consumption limitation, optional functions implanted in OBELIX will only be available at the outer layers. The first version of OBELIX is expected to be submitted at the beginning of 2024. More details about this ASIC are to be found in the Conceptual Design Report for the project which should be published early 2024. In parallel, progresses are currently done on the integration effort, as we are working on the first prototype for the inner layers of VTX and on an advanced prototype for the outer layers of VTX (including support material and flex print cable).

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