PROCEEDINGS OF SCIENCE

Recent results from MAPS prototypes for ITS3

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The present Inner Tracking System (ITS2) of the ALICE Experiment will be upgraded during the LHC Long Shutdown 3 (LS3). The upgrade foresees the replacement of the three innermost layers with a truly cylindrical vertex detector, the ITS3. Such tracker will be composed of two half barrels, comprising three self-supporting cylindrical half-layers, each made of two large-area (O(10×26 cm^2)) ultra-thin (≤50 µm) bent stitched Monolithic Active Pixel silicon Sensors (MAPS) fabricated in a 65 nm CMOS process. This novel technology will allow for an unprecedented low material budget of 0.05 %X/X_0 per layer, strongly improving the tracking efficiency and the pointing resolution, especially for low-momentum particles.

An extensive campaign to validate the sensor technology through characterisation both in the laboratory and with in-beam measurements is ongoing. For this purpose, multiple test structures were included in the first test production (MLR1) to be tested: Analog Pixel Test Structure (APTS), Circuit Exploratoire 65 (CE65) and Digital Pixel Test Structure (DPTS). Excellent performance in terms of detection efficiency (>99%), spatial resolution (3-4 µm) and response to X-rays were achieved. Moreover, good performance achieved on irradiated APTS and DPTS proved the 65 nm CMOS process tolerant far beyond 1×10^{13} 1 MeV n_{eq} cm^{-2} (NIEL) and 10 kGy (TID), expected for the ALICE ITS3 operating environment.

This contribution will describe the different test structure flavours and the most recent results from laboratory and beam test measurements will be presented.

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1. Introduction

The Inner Tracking System (ITS2) of ALICE (A Large Ion Collider Experiment) at the Large Hadron Collider (LHC) is a tracker with 7 layers based on Monolithic Active Pixel silicon Sensors (MAPS) [1]. It will undergo an upgrade [2] during the LHC LS3 (Long Shutdown 3) that foresees the replacement of the three innermost layers with an innovative ultra-light and flexible tracker, the ITS3. The layout of such a detector (fig. 1) includes two half barrels, each composed of three truly cylindrical layers. Each half layer will consist of a single large-area (O(10×26 cm^2)) ultra-thin (≤50 µm) bent stitched Monolithic Active Pixel silicon Sensor (MAPS) fabricated in a 65 nm CMOS process and held in place around the beam pipe by ultra-light carbon foam support structures.

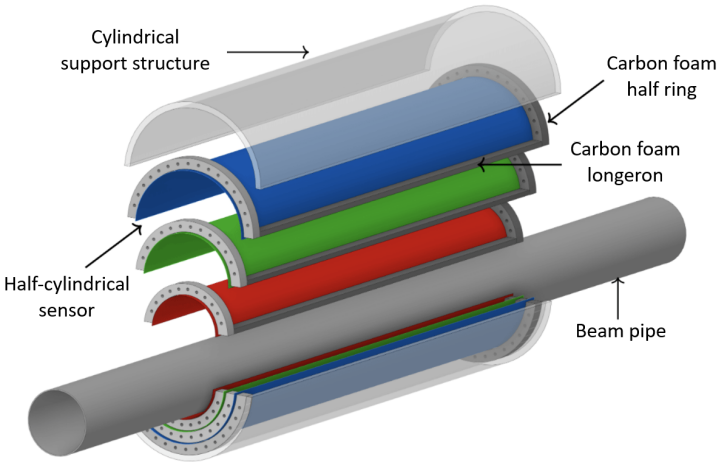


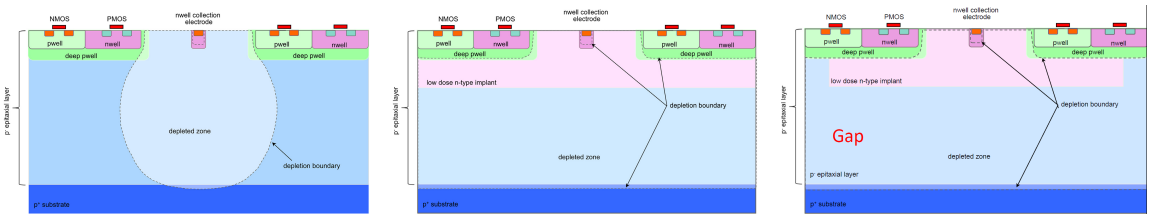
Figure 1: The ITS3 layout, with three layers each composed of two single large-area (O(10×26 cm^2)) ultra-thin (≤50 µm) bent MAPS detectors held in position by ultra-light carbon foam supports.

The novel approach will minimize the impact of the support and cooling structures and implement in-silicon powering and data transfer, thus targeting an unprecedentedly low material budget of 0.05% X/X$_0$ per layer. This feature, combined with the placement of the detector closer to the beam pipe (minimum radius of 1.8 cm) and the reduction of the pixel pitch (15 - 25 µm) will strongly improve the tracking efficiency and the pointing resolution, especially for low-momentum particles.

An extensive campaign to validate the sensor technology for the ITS3 is ongoing. More details on sensor prototypes and characterisation results are given in the following sections.

2. The prototypes for the ITS3

The first test sensor production, Multiple Layer Reticle 1 (MLR1), was submitted in 2020 and received in September 2021. It is the first submission of prototypes fabricated in the Tower Partners Semiconductor Co. (TPSCo) [3] 65 nm CMOS imaging process for MAPS silicon detectors. This technology is under study in collaboration with the CERN EP R&D [4] on monolithic sensors. The sensors realized in the 65 nm CMOS imaging process are expected to have a high radiation hardness and a low power consumption. Moreover, the small dimension of the in-pixel transistors allows



(a) Standard process **(b)** Modified process **(c)** Modified process with gap

Figure 2: Section of a MAPS pixel for each of the three process option explored with the prototypes included in the MLR1 test production.

for reducing the pixel pitch, resulting in a 2D spatial resolution of 5 µm. Finally, the large size of the produced wafers (Ø 300 mm) allows for meeting the ITS3 sensor dimensional requirements (O(10×26 cm^2)).

Three process options were explored [5, 6], differing in the doping profile. The *standard* process (fig. 2a) is the same implemented in the widely characterised ITS2 ALPIDE [7] sensor. The *modified* process (fig. 2b) features an additional low-dose n-type implant between the in-pixel electronics and the epitaxial layer, which allows for the complete depletion of the epitaxial layer, resulting in a faster and more efficient charge collection with respect to the standard process. The charge sharing between adjacent pixels is reduced as well. The *modified with gap* process (fig. 2c) features an additional gap in the low dose n-type implant at the edges of the pixels.

Multiple 50 µm thick test structures were included in the MLR1 to study different aspects of the 65 nm CMOS imaging process. The results presented in this contribution regard the Analog Pixel Test Structure (APTS), the Circuit Exploratoire 65 (CE65) and the Digital Pixel Test Structure (DPTS).

The APTS features a 6×6 pixel matrix with a pixel pitch of 10, 15, 20 or 25 µm. It has an analogue readout of the central 4×4 pixel matrix and was realised with two output buffer versions: Source Follower (SF) and Operational Amplifier (OA). The main goal of the APTS is to explore different pixel designs. The CE65 [8] features a 64×32 pixel matrix with a pixel pitch of 15 µm or a 48×32 pixel matrix with a pixel pitch of 25 µm. Its readout is based on a rolling shutter architecture with 50 µs integration time. The main goal of the CE65 is to explore pixel matrix uniformity and to study the rolling shutter readout performance in a 65 nm CMOS imaging process sensor. The DPTS [9] features a 32×32 pixel matrix with a pixel pitch of 15 µm. It has an asynchronous digital readout which retains the time-encoded pixel position and the analog signal Time-over-Threshold (ToT). The main goal of the DPTS is to study the in-pixel front-end.

3. Test results

APTS, CE65 and DPTS are being characterised through a wide test campaign both in the laboratory and with in-beam measurements. In this section the main results are presented.

3.1 Process selection and radiation hardness with the APTS SF

Three APTS SF, one for each process option (i.e. standard, modified, modified with gap), were illuminated with a ^{55}Fe radioactive source. The measured spectra are compared (fig. 3a) to assess

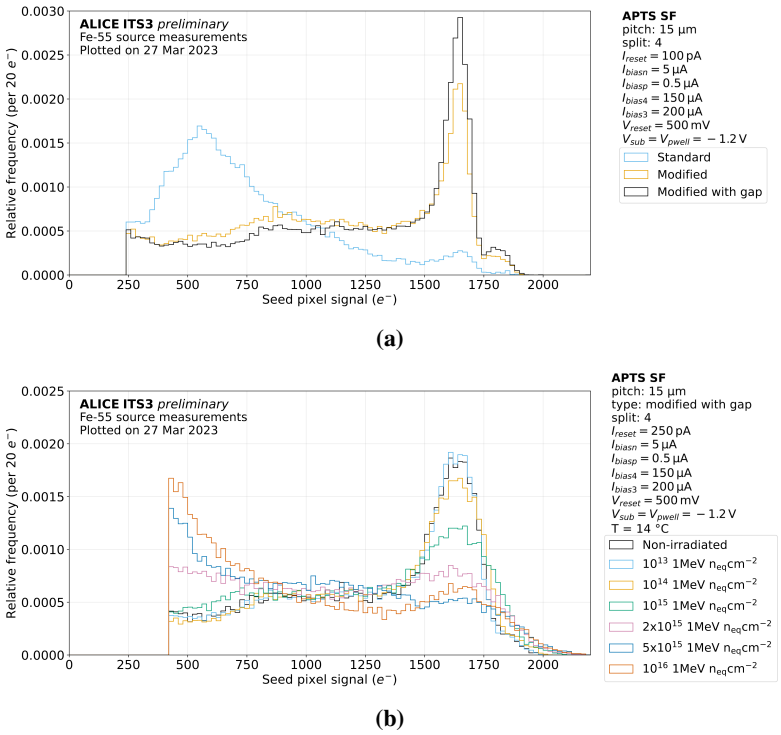


Figure 3: Comparison of ^{55}Fe source spectra measured with three APTS SF one for each process option (a) and comparison of ^{55}Fe source spectra measured with APTS SF irradiated with different level of Non-Ionising Energy Loss (NIEL) (b).

the performance of each process. Relevant charge sharing is observed for the standard process, while it is reduced for the modified and modified with gap processes. The best performance in terms of yield of the two characteristic emission peaks of the source is observed for the modified with gap process, which was then selected as the most performing process among the three.

The ^{55}Fe spectra measured with multiple APTS SF realised with the modified process and irradiated with different levels of Non-Ionising Energy Loss (NIEL) radiation were compared to assess the radiation hardness of these test structures (fig. 3b). The spectrum measured with the APTS irradiated with a level of NIEL radiation of 10^{13} 1MeV n_{eq} cm^{-2}, equal to the ITS3 requirement, looks unmodified with respect to the spectrum measured with the non-irradiated APTS. Moreover, the APTS irradiated up to 10^{16} 1MeV n_{eq} cm^{-2} is still operational despite the relevant increase in charge sharing.

3.2 Radiation hardness with the DPTS

In-beam measurements were done at the CERN PS with 10 GeV/c positive hadrons with DPTS realised in the modified with gap process to study the radiation hardness of the prototypes to NIEL radiation and Total Ionising Dose (TID) radiation. A detection efficiency (fig. 4a) higher than 99% was measured in a wide range of applied threshold in particular, for the DPTS irradiated with the combined TID and NIEL levels expected for the ITS3 (10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}). An efficiency of 99% was measured with the DPTS irradiated with a NIEL radiation level of

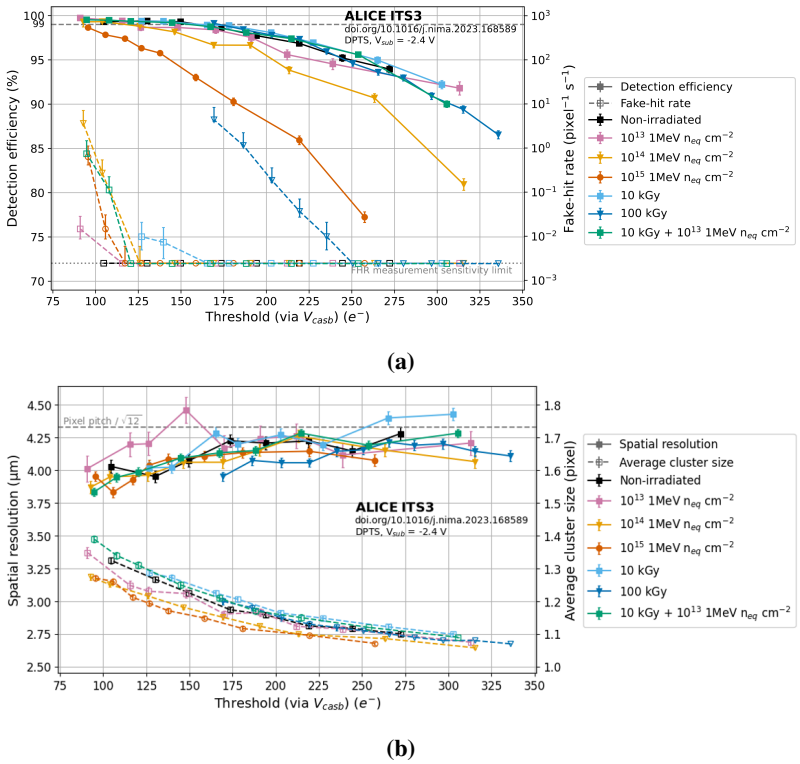


Figure 4: Detection efficiency (a) and spatial resolution (b) measured with 10 GeV/c positive hadrons at the CERN PS with different DPTS irradiated with multiple level and type of radiation.

10^{15} 1MeV n_{eq} cm^{-2}, which is two orders of magnitude higher than expected for the ITS3. A spatial resolution (fig. 4b) lower than the binary resolution was measured for all the DPTS, unaffected by the radiation type and level.

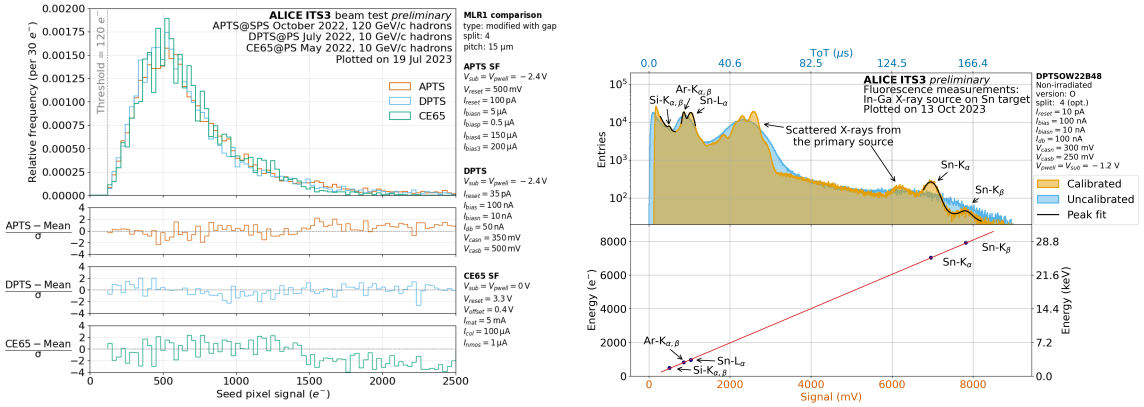
3.3 Energy-loss measurements

The Minimum Ionising Particles (MIP) energy loss was measured with beam tests for APTS, CE65 and DPTS. A comparison of the corresponding energy-loss distributions is shown in fig. 5a. The residual difference for the three test structures are centered in zero, thus proving the consistency and reliability of the measurements.

An X-ray Fluorescence (XRF) measurement was done with the DPTS, using an In-Ga X-ray source illuminating a tin target. The fluorescence spectrum, measured by exploiting the ToT measurement capability of the DPTS, allowed for the energy calibration of the DPTS ToT response up to 28.8 keV, corresponding to the Sn Kβ emission. Moreover, it demonstrated the DPTS energy response linearity up to 28.8 keV.

4. Conclusions

An innovative vertex detector, the ITS3, is foreseen to be installed in 2026 for the ALICE Experiment. It will be made of large-area (O(10×26 cm^2)), ultra-thin (≤50 µm), flexible, bent (minimum radius 1.8 cm) MAPS detectors. The activities towards the ITS3 are on schedule. The



(a) **(b)**

Figure 5: Left: MIP enery-loss distribution comparison between APTS, CE65 and DPTS. Right: fluorescence tin target spectrum measured with the DPTS.

65 nm CMOS process has been validated by characterising multiple test structures included in the first production (MLR1). Three doping profiles were explored: standard, modified and modified with gap. The modified with gap process was demonstrated to be the most performing in terms of charge collection efficiency when illuminated with an ^{55}Fe source. A NIEL radiation hardness up to the expected level for the ITS3 of (10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}) was verified for both APTS and DPTS prototypes: an unmodified ^{55}Fe spectrum with respect to the non-irradiated sensor was measured for the APTS and a detection efficiency higher than 99% in a wide range of applied threshold was measured for the DPTS. The energy response to MIP particles is consistent between the APTS, CE65 and DPTS, demonstrating the reliability of the prototypes. Moreover, the linearity of the energy response of the DPTS was verified with XRF measurements up to 28.8 keV. In the meantime, the second sensor production, named Engineering Run 1 (ER1), including the first large-area sensors realised with the stitching technique, has been received, and the characterisation tests are ongoing.

The technology that is currently under development for the ITS3 will be the starting point for the new tracker of the future experiment ALICE 3 [10], proposed for the LHC Run 5 and Run 6.

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