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Overview of the ATLAS High Granularity Timing Detector: project status and results

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The increase of the particle flux at the HL-LHC scenario, with instantaneous luminosities up to 7.5×10^{34} cm^{-1}s^{-2}, will have a severe impact on the ATLAS detector reconstruction and trigger performance. This is particularly challenging in the detector end-cap and forward region, where the liquid Argon calorimeter has coarser granularity and the inner tracker has poorer momentum resolution. A High Granularity Timing Detector (HGTD) will be installed in front of the LAr end-cap calorimeters to help with pile-up mitigation, as well as to provide a measurement of the luminosity. Thus, the HGTD is introduced to assist the new all-silicon Inner Tracker (ITk) in the pseudo-rapidity $2.4 < |\eta| < 4.0$ range, adding the capability to measure charged-particle trajectories in time, as well as space. Two silicon-sensor double-sided layers will provide precision timing information for minimum-ionising particles with a resolution as good as 30 ps per track, to help disentangle tracks from different vertices in the same bunch crossing. Readout cells have a size of 1.3 mm $\times$ 1.3 mm, leading to a highly granular detector with 3.6 million channels. Low Gain Avalanche Detectors (LGAD) technology has been chosen, as it provides enough gain to reach the large signal over noise ratio needed. The requirements and overall specifications of the HGTD will be presented, as well as the technical design and the project status. The on-going R&D effort, carried out to study the sensors, the readout ASIC, and other components, supported by laboratory and test beam results, will also be presented.

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1. Introduction

The High Luminosity upgrade of the LHC (HL-LHC) will increase the instantaneous luminosity to L$\simeq 7.5 \times 10^{34}$ cm^{-1}s^{-2} [1]. This entails an average of 200 interactions per collision, a notably increased pile-up that has forced the upgrade of many parts of the ATLAS detector. Among them, the fully renewed all-silicon tracker (ITk) [2] will be able to maintain excellent tracking performance in the central region of the detector. To enhance the pile-up mitigation in the forward region ($|\eta| > 2.4$), a new detector, the High Granularity Timing Detector (HGTD) [3], is planned to be installed in the end-cap areas (see Figure 1) .

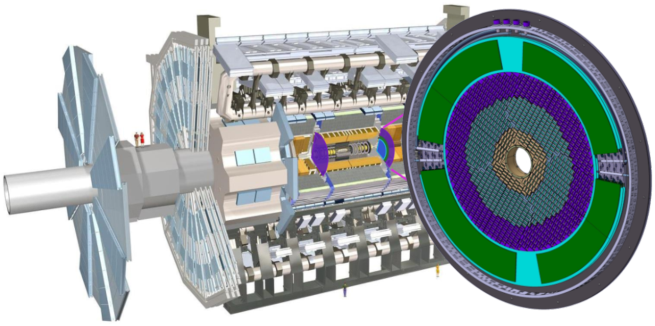


Figure 1: Position of the HGTD within the ATLAS Detector. The HGTD acceptance is given by the detector radius of 120 mm and 640 mm at a position of z= ±3.5 m along the beamline, on both sides of the detector.

HGTD will provide timing information to minimize the impact of pile-up, as well as deliver bunch by bunch luminosity information. The detector targets at a time resolution of 30 ps per track at the beginning of the HL-LHC and 50 ps after a fluence of 2.5×10^{15} n_{eq}/cm^2. It will cover the forward region with $2.4 \leq |\eta| < 4.0$ and it is composed of two double sided layer disks mounted on a cooling plate; each active layer on the disk has 3 rings with modules made of silicon sensors. The modules contain two Low Gain Avalanche Detectors (LGAD), selected for the HGTD on account of their excellent timing properties. Within the module, each sensor is bump-bonded to a front-end ASICs (ALTIROC), specifically designed for the HGTD, to record the timing and hit information of the LGAD signals. A module is thus composed by two LGAD-ALTIROC hybrids, connected through wire-bonds to a single flexible PCB, that relays the collected information to the peripheral electronics. From the peripheral electronics, this information is sent to back-end servers through optical links.

These proceedings will briefly describe the R&D and current status of the LGAD sensors and ALTIROC ASICs in Sections 2 and 3, respectively, whereas the status of the HGTD modules and support units is summarized in Section 4.

2. LGAD sensors for HGTD

The LGADs are pixelated planar n-on-p silicon sensors with a buried multiplication layer, which provides a moderate gain on the collected signal [4]. The multiplication layer is formed by the addition of a highly doped p-layer below the n-type electrode, so that the electric field in that

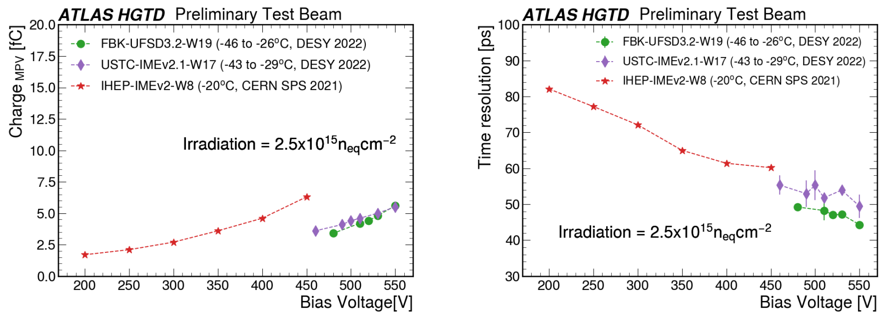


Figure 2: Test Beam performance of Carbon-enriched LGAD sensors irradiated at the EoL fluence of 2.5×10^{15} n_{eq}/cm^2: Left: Charge collection; Right: Time Resolution

region is enhanced to enable impact ionization on the crossing charge carriers. When a charged particle crosses the detector, an initial current is induced by the drift of the electrons and holes generated in the silicon. Electrons reaching the multiplication layer generate new electron-hole pairs and the resulting current is enlarged by their drift towards the electrodes. This charge amplification is referred as the gain of the LGAD and it is the key ingredient to allow a reduction on the sensor thickness, while keeping the signal amplitude comparable to that obtained with thicker conventional sensors, and altogether leading to a better time resolution.

For the HGTD, 50 μm-thick LGAD sensors with a pixel pad size of 1.3 mm $\times$ 1.3 mm have been selected as a baseline, due to occupancy requirements: smaller pads yield to better spatial resolution, but also increase the amount of relative inactive area, since the inter-pad gap has no gain. HGTD LGAD sensors have 15 $\times$ 15 pixels and target at a time resolution per track of 30 ps, with a charge collection of at least 10 fC per MIP before irradiation. At the end of life (EoL) of the sensors, after having received a 1-MeV neutron equivalent fluence of 2.5×10^{15} cm^{-2}, they are expected to keep the charge collection above 4 fC, with a time resolution better than 50 ps per track.

LGAD performance has been extensively studied during the R&D phase [5]. Sensor technologies from different manufacturers were tested looking for the best performance in terms of time resolution, charge collection or hit efficiency, among other aspects. Radiation hardness is one of the main challenges for LGAD sensors, as it has been observed [6] that the charge collection reduction, typically observed in all the irradiated silicon sensors, is accompanied in the LGADs with a reduction of the gain. Nevertheless, the addition of carbon in the multiplication layer helps to mitigate the acceptor removal, responsible for the gain reduction. The performance of Carbon-enriched sensors has been thoroughly studied in beam tests carried out at DESY and CERN [7]. As shown in Figure 2, the charge collection and time resolution, together with the hit efficiency (not included in this proceedings for the sake of concision), are still able to meet the HGTD requirements, even at the EoL expected fluence.

In addition, EoL beam tests [8] helped to uncover a failure mode, associated to a Single Event Burnout (SEB) that takes place when the irradiated LGADs are operated at very high voltage bias. The minimum bias at which the SEB was observed for different technologies is represented in Figure 3 as a function of the sensor thickness. About 80 samples of different flavours were analyzed to obtain a fit which set the critical electric field for the SEB occurrence at 12.1 V/μm.

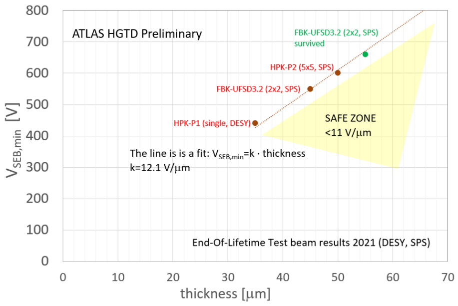


Figure 3: Minimum voltage bias at which the Single Event Burnout was observed as a function of the sensor thickness. A safe operation zone (yellow), in which the SEB does not take place, has been delimited for the irradiated LGADs.

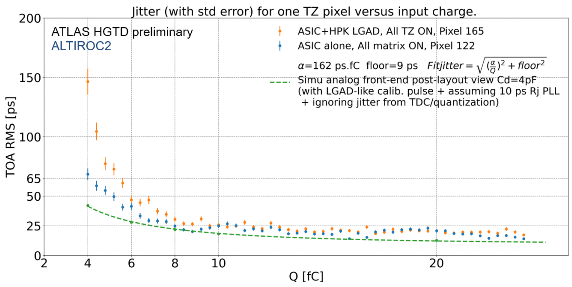
This allows the delimitation of a safe operation zone, in which the electric field is hold below 11 Vμm. Carbon-enriched LGADs, that experience lower degradation in their performance and therefore need lower voltage bias, can be operated within the safe operation zone even under the EoL irradiation conditions.

3. The ALTIROC HGTD ASIC

The ALTIROC is the read-out ASIC specifically designed to interface the HGTD LGADs. Accordingly, it has 225 channels that are bump bonded to the corresponding pixels of a full size sensor. Each channel contains an analog front-end that features a pre-amplifier and a discriminator to detect the LGAD signals. The discriminator output leads to two Vernier Time-to-Digital converters that register the Time-of-Arrival (TOA) and Time-over-Threshold (TOT) of the signal. These timing data, together with a hit flag (eventually used to calculate the luminosity per bunch crossing), are stored in digital registers and e-link transmitted upon a trigger reception from the internal layers of ITk (L0 and L1).

The timing requirements for ALTIROC are quite strict. It needs to reach a jitter of 25 ps at 10 fC input charge, which can be increased up to 65 ps at 4 fC. These charge levels represent the expected charge collection of the sensors at the beginning and at the end of their lifetime. The ASIC also needs to trigger the discriminator at a threshold of 2 fC, while maintaining a high efficiency.

In 2022, the ALTIROC2 version of the ASIC was produced, featuring most of the final requirements. It has all 225 channels, two pre-amplifier designs (voltage and transimpedance), local digital memory and a data serializer for communication. The discriminator threshold, TOA, TOT, jitter and other important requirements were verified through an extensive campaign of tests (e.g. in [9]). The tests also included measurements on hybrids, produced by bump-bonding the ALTIROC2 chips with full-size LGAD sensors and their performance was compared with that of the bare ASICs. Figure 4(a) shows that the TOA jitter of the hybrids was higher than that of the bare chip and did not meet HGTD requirements. In the same way, it can be seen in Figure 4(b) that the minimum threshold obtained for the hybrids was only 3.8 fC, while the performance of the bare ASIC met the requirements. After many tests, parasitic capacitances between the sensors and the pre-amplifier were identified as the most likely cause of these discrepancies.



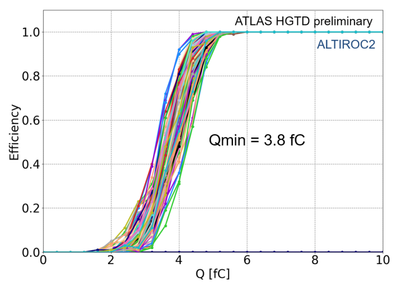


Figure 4: ALTIROC2 performance: (Left) TOA jitter on a single channel for a simulation, a bare ALTIROC2 and an ALTIROC2-LGAD hybrid at various levels of injected charge; (Right) Efficiency of all the transimpedance (TZ) channels on an ALTIROC2-LGAD hybrid at various levels of injected charge.

The next generation of the ASIC (ALTIROC3) has been recently released. This version is the final rad-hard prototype before starting the production. Among its main features, ALTIROC3 only includes the transimpedance amplifier and incorporates a correction of the pre-amplifier voltage drops along the columns, which addresses the limitation of ALTIROC2. The first tests with ALTIROC3 bare ASICS and hybrids are presently on going and the outcome will be released in the next months.

4. Assembly and performance of prototype modules

During the last year, the first HGTD full modules have been produced. Each of these modules feature two ALTIROC-LGAD hybrids mounted and wire-bonded on a single flexible PCB (flex), for the HV biasing of the sensor and the ASIC readout and powering (see Figure 5(a)). The module assembly is taking place in six different institutes: three in Europe (IFAE, UJG-Mainz and IJClab), two in China (IHEP and USTC) and one in Morocco (MAScIR). The assembly methods differ from site to site, but all target at the same specifications. In this sense, the collaboration is coordinating an extensive work on standardizing and unifying criteria, in particular with respect to the final metrology of the modules. So far, all the prototype modules included ALTIROC2 hybrids, with sensors coming from different vendors, with slightly different sizes and thicknesses. This leads to a small variability on the overall module dimensions from site to site. Several flex versions, all designed for ALTIROC2, were also explored. A new module flex design is being developed for the ALTIROC3 and the assembly of the first ALTIROC3 modules will take place during the next few months.

Up to date, the assembly sites have produced more than 60 HGTD modules and they have been tested under different conditions. The tests targeted at the threefold objective of assessing the quality of the assembly process, developing proper procedures and hardware and software tools for the tests, as well as evaluating the performance of the modules itself. In this sense, there have not been observed relevant discrepancies in the performance of the module hybrids with respect to that observed in the single hybrids mounted on PCBs. Most modules were fully configurable and the threshold could be tuned below 4fC. MIP collection in each of the channels was also analyzed with the aid of an Sr-90 source. As way of example, Figure 6 shows the outcome of a source scan. For modules assembled with baseline hybrids, a 100% bump connection is typically observed.

The modules need to be attached to support units so as to be mounted on the HGTD cooling plate. The loaded support units are called detector units. HGTD will have 13 unique detector unit designs per side, that will have different configurations and hold different amount of modules. This number was chosen to optimize the assembly procedure and minimize gaps between readout rows. The modules on the detector units communicate with the peripheral electronics through long flexible PCBs called flextails, which carry the power, HV bias, data and control signals. The flextails features are being thoroughly studied, but they lay out of the scope of this review (see instead [10]). In the same way, the loading of modules on detector units and their connection to the peripheral electronics is to be evaluated through the HGTD demonstrator program. It will consist of 54 modules mounted on detector units connected to a prototype peripheral electronic board. The structure will be mounted on a cooling plate and connected to a backend server. The goal is to read all 54 modules successfully and maintain them at a stable temperature. The demonstrator is now under construction and the first detector unit (Figure 5(b)) has been already loaded with 12 HGTD modules. The project will continue along the next months.

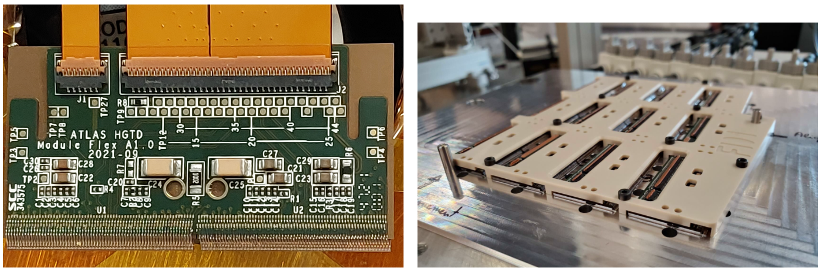


Figure 5: Left: Prototype HGTD module for the ALTIROC2 version of the hybrids. Right: Demonstrator Detector Unit loaded with 12 HGTD modules

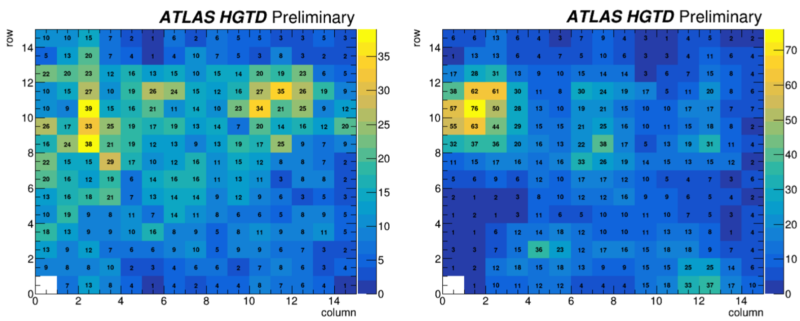


Figure 6: Occupancy map measured with Sr-90 source on the two hybrids of a full HGTD module. Two 15×15 FBK LGADs hybridized to two ALTIROC2 readout chips on a module flex PCB. HV = 150 V. Target threshold = 25 DAC (10 fC). Note that pixel (0,0) was intentionally not bump-bonded to enable other studies.

5. Conclusions

HGTD is a new detector for ATLAS that will add precision timing information to tracks in the forward region during the HL-LHC era. It will improve the pile-up rejection and thus enhance the object reconstruction in harsh environments. The goal is a 30 ps track timing resolution that can rise up to 50 ps at the highest estimated fluence at the sensors end-of-lifetime. Dedicated R& D test campaign helped to establish that LGAD sensors with carbon infused gain layers can meet the performance requirements even under the hardest fluence conditions. The first full size prototype version of the readout ASIC, ALTIROC2, was manufactured and thoroughly tested, both as a bare chip and after having been hybridized with the sensors. The first HGTD modules, which attach and connect two ALTIROC2-LGAD hybrids on a single flexible PCB, are being assembled and tested, as well, and they have already started to be loaded on dedicated detector units for a full demonstrator that integrates the cooling system and the DAQ readout chains with real modules and electronics. Modules with the recently released rad-hard version of the ASIC, ALTIROC3, will be also included in the HGTD demonstrator.

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