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Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Maheyer Jamshed Shroff[a,*] **,on behalf of the ATLAS Liquid Argon Calorimeter Group**

[a] *University of Victoria, Victoria, Canada*

E-mail: maheyer.jamshed.shroff@cern.ch

A new era of hadron collisions will start around 2029 with the High-Luminosity LHC which is designed to collect ten times more data than what has been collected during 10 years of operation at LHC. This will be achieved by higher instantaneous luminosity at the price of a higher number of collisions per bunch crossing. In order to withstand the high expected radiation doses and the harsher data taking conditions, the ATLAS Liquid Argon Calorimeter readout electronics is being upgraded. The electronic readout chain is composed of four main components. 1) New front-end boards will amplify, shape, and digitise the calorimeter's ionisation signal using two gains over a dynamic range of 16 bits and 11 bit precision. 2) New calibration boards will inject precise calibration of all 182468 channels of the calorimeter over a 16 bit dynamic range. 3) New ATCA compliant signal processing boards ("LASP") will receive the detector data at 40 MHz, where FPGAs connected through lpGBT high-speed links will perform energy and time reconstruction. In total, the off-detector electronics receive 345 Tbps of data via 33000 links at 10 Gbps. For the first time, online machine learning techniques are being considered for use in these FPGAs. A subset of the original data is sent with low latency to the hardware trigger system, while the full data are buffered until receiving of trigger accept signals. The latest status of the development of the board and the firmware is shown. 4) A new timing and control system, "LATS", will synchronise the aforementioned components. Its current design status will also be shown.

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1. Introduction

The current progress is discussed for the upgrade of the readout electronics of the ATLAS Liquid Argon (LAr) calorimeter for the High-Luminosity Large Hadron Collider (HL-LHC) era, which is expected to begin in 2029.

The ATLAS Liquid Argon Calorimeter measures the energy and timing of photons, electrons, and hadrons that are produced by proton–proton collisions in the Large Hadron Collider (LHC) with a signal sensitivity able to detect minimum ionizing muons. It is a set of sampling calorimeters comprised of a total of 182468 readout cells using liquid argon as the active material and absorbers consisting of lead, copper or tungsten[1].

The LAr readout electronics system is separated into on- and off-detector components. The on-detector electronics shapes and samples the cells at the LHC bunch crossing (BC) frequency of 40 MHz, and sends a digitised pulse to the off-detector electronics where it is processed to extract energy and time for each cell. This information is then propagated to the trigger and the data acquisition (DAQ) systems.

During the HL-LHC era, ATLAS will receive an instantaneous luminosity of up to 7×10^{34} cm^{-2}s^{-1} (7 times the original LHC design), corresponding to approximately 200 simultaneous collisions expected in each bunch crossing[2]. In this environment, differentiating signal from noise is harder, and therefore the trigger needs more granular shower information. The ATLAS trigger system is being upgraded as well to a new architecture with 10 μs latency and a rate of 1 MHz at the hardware trigger level[3].

A full upgrade of the LAr main readout chain is required to not only accommodate the high trigger rates needed, but also because the current system will not survive will the full HL-LHC radiation dose. The forseen design for the upgraded LAr readout is being built, with cell data for each bunch crossing digitised and sent to the off-detector electronics, resulting in no on-detector pipeline.

2. LAr upgrade Readout components

Figure 1 shows the architecture of the full LAr calorimeter readout scheme for ATLAS in the HL-LHC. The physics goals of the experiment dictate the specifications for the system. The readout electronics handles a large dynamic range of energy deposits: the low-end is defined by the energy deposit of muons at the minimum ionization (MIP) in one cell (50 MeV), and the high end is approximated as 3 TeV which could come from electrons or photons produced in the decay of a new particle with mass $O(10)$ TeV. Nonlinearity requirements are also imposed to ensure accurate measurements, specifically < 0.1% for cell energies up to approximately 300 GeV. Components must also function for the full expected HL-LHC radiation dose, corresponding to a total ionizing dose of 1400 Gy (including a safety factor of 1.5).

2.1 On-detector electronics

The on-detector LAr electronics consists of second-generation front-end board (FEB2) and the calibration boards. Each of the 1524 FEB2 reads out up to 128 channels, and each of the 122 calibration boards contains 128 input lines. (A line injects signal to several cells simultaneously).

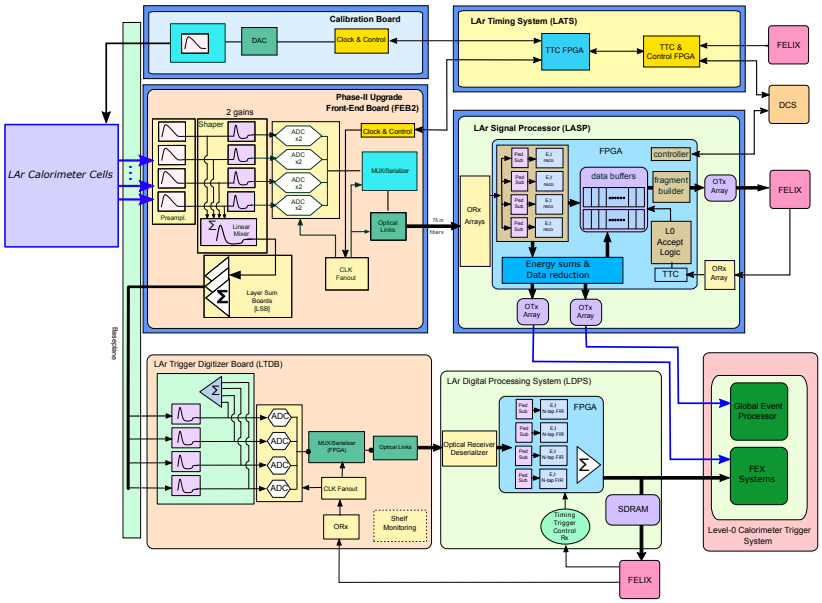

Figure 1: Layout of the LAr readout in the HL-LHC, including all on- and off-detector electronics. The LTDB and the LDPS are items that have been already commissioned and installed and will serve as legacy components in HL-LHC operation.

2.1.1 Calibration Board

The calibration board provides a pulse of known amplitude and shape which is directly injected into the calorimeter cells. The system must satisfy an integral nonlinearity below 0.1%, a fast rise time below 1 ns, 16-bit dynamic range, and must be radiation hard up to 180 kRad. A total of 122 boards with 128 input lines each are needed to calibrate the 182,468 calorimeter cells. The calibration system consists of 2 custom ASICs. A CLAROC creates a pulse by opening a high-frequency switch. Because the dynamic range of the pulse may be up to 7.5 V, this chip is designed in 180 nm XFAB HV-CMOS technology. The second ASIC is the LADOC which is a 16-bit DAC that is used to control the switch, built in 130 nm TSMC technology. Tests with the ASICs indicate that they meet the nonlinearity specifications, and radiation hardness tests are currently in progress. A 32-channel prototype board, CABANE, is being fabricated which measures cross-talk between channels and tests the integration between the two ASICs.

2.1.2 Front-end board

The FEB2 boards perform analogue processing and digitisation of the calorimeter signals. First, the signal is amplified and shaped and split in two linear gain scales. Then an ADC digitises the low and the high gain at 40 MHz, which is then serialized, multiplexed and sent off-detector via optical links. The FEB2 is made of 32 Preamplifier/shaper ASICs, 32 ADC ASICs, 24 serializer chips (lpGBT) and 8 optical modules (VTRX+). In total each FEB will have up to 22 output links sending data at 10.24 Gbps each

Preamplifier-Shaper The preamplifier/shaper (PA/S) chip is the first chip in the readout chain. The signals are first amplified, shaped into a bipolar pulse shape using a CR-$(RC)^2$ circuit,

and then split into two overlapping gain with a gain ratio of around 23. The generated differential outputs are passed to both the next pipeline in the readout chain, as well as to the L0 trigger (this is the legacy path that is used for redundancy). PA/S on the FEB2 uses the ALFE, which is the prototype custom ASIC built in 130 nm CMOS TSMC technology with 4 channels per ASIC. It has a tuneable input impedance to match the varying cell size across the calorimeter, as well as tuneable time constants for the shaping function. ALFE testing shows it satisfies the specifications of integral nonlinearity < 0.1%, crosstalk (< 20 mV for 50 Ω input impedance) and radiation testing also revealed that the ALFE maintains good performance after a 12 kGy dose (8 times larger than the anticipated dosage).

ADC Signals from the PA/S are then sampled and digitised by the ADC. The ADC digitises signals on a 14-bit dynamic range with two gains to cover the required 16-bit dynamic range. A custom 65 nm CMOS ASIC called the COLUTA is designed to process 8 LAr channels for this task. The COLUTA consists of a 3-bit multiplying DAC, followed by a 12-bit Successive Approximation Register (SAR), pipelined with a Digital Data Processing Unit (DDPU) which applies calibration bit weights and transmits the digitised data. Tests with COLUTA consistently have an effective number of bits (ENOB) greater than 11, as required by the specification. Other specifications on nonlinearity and radiation tolerance are also met.

FEB2 Preprototype - Slice test board Integration of earlier versions of the ALFE and COLUTA are used in a so-called "slice-test board", showcasing functionality for 32 channels (instead of the 128 channels that will be the real input to the FEB2). In addition to the ALFE and the COLUTA, the slice-test board also contained lpGBTs and VTRX+ that are used for both data transmission as well as control.

The slice test board has successfully demonstrated full digital functionality of configuring all the chips on board. The slice test also demonstrated the redundancy of bidirectional CLK and control links and slow control and monitoring functionality. Reconstruction ability has also been studied on the board where LAr pulses of a variety of amplitudes are read out. Energy resolution σ_E/E for the highest energy pulses is also tested to be well below the specification of 0.25%.

A full-scale 128-channel prototype board is now submitted for fabrication at which point power distribution tests can be performed.

2.2 Off-detector electronics

The off-detector electronics has 30 LAr Timing System (LATS) boards and 278 LAr Signal Processor (LASP) boards. The LASP handles the digital signal processing and sends output data to the Trigger and Data acquisition system. The LATS provides the Timing, Trigger and Control interface (TTC) to the on-detector electronics. The off-detector electronics will be housed in the counting room of the ATLAS Experiment and will be shielded from collision radiation. Data between the on-and off-detector will primarily be transmitted using the lpGBT protocol.

2.2.1 LAr Timing System

The LATS distributes the TTC signals to the FEB2 and calibration boards and handles the configuration and monitoring. A dedicated ATCA board, called the LATOURNETT, is designed

for this and can control up to 72 boards simultaneously. It consists of a matrix of 12 Intel Cyclone 10 FPGAs, which transmit and receive control/monitoring signals. Another Intel Cyclone 10 FPGA is also present for centralized control. A first board prototype is ready, and tests on the board are in progress as well as the firmware that will run on the FPGAs.

2.2.2 LAr Signal Processor

The LASP receives data from the FEB2 and applies digital filtering algorithms to compute the energy and time of the pulse. Each LASP blade will receive data from 6 FEB2s, and will have two onboard Intel Agilex I-Series FPGAs, an Intel MAX10 FPGA, and a CERN IPMC, the latter two used for board monitoring and control. Processed LASP data are sent to the Trigger and DAQ. Accompanying the LASP is a Smart Rear Transition Module (SRTM), which offloads some of the High-speed serialisation and encoding tasks and also does monitoring and control. The SRTM will fit into the back plane of the ATCA crate, with the LASP blade fitting on the front side. Multiple LASP test boards have been fabricated and distributed to labs around the world for detailed hardware validation and firmware development.

Machine Learning Real-time digital signal processing With increased pileup from the HL-LHC, the energy and timing resolution would be poorer resulting in a worse performance of the trigger. Both in-time pileup which comes from multiple proton collisions within the same BC, and out-of-time pileup consist of energy that is leftover in the calorimeter from previous BCs which accumulates because the LAr pulse signal is approximately 25 BCs long, can degrade performance[4]. For this reason, machine learning (ML) algorithms executed online by the FPGA itself are being studied.

Architectures being studied include convolution neural networks (CNN), which are separated into two tasks: a tagging layer that detects energy deposits 3σ above the electronic noise and produces a detection probability, and an energy reconstruction layer that reconstructs the amount of energy deposited in each cell.

Recurrent neural networks (RNN) and long short-term memory (LSTM) architectures are also being studied. These model the data as a sequence of BCs, which helps to better account for the effects of out-of-time pileup. The LSTM is used with both single BC inputs and a sliding window technique that uses up to four inputs from the current pulse and one from the previous pulse. The Vanilla RNN can only be used with sliding window inputs as it does not have sufficient complexity to manage information over long periods of time[4].

Figure 2 shows the energy reconstruction performance for the optimal filtering and the various ML algorithms studied. All ML-based reconstructions outperform the legacy method (Optimal Filter, OF) in both accuracy and precision. The final model selection would be a trade-off between sufficient performance and FPGA resource usage.

3. Integration

As pre-prototype boards are developed, there is work to try to integrate these boards. A test setup at CERN interfaces and connects the on-detector slice-test board and the LASP test boards. Using current ATLAS TTC and DAQ services, a small-scale readout chain has been demonstrated:

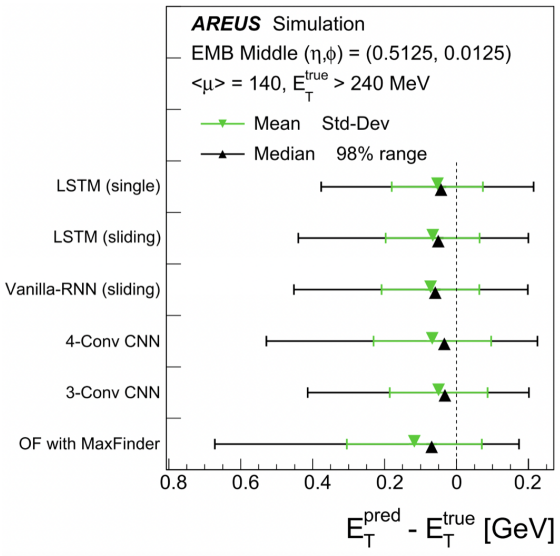

Figure 2: Reconstruction performance of the optimal filtering method and the various ML algorithms studied[4].

data from the FEB2 is received by the LASP, which is then transmitted to the DAQ, all running with a centralized TTC clock.

A larger scale readout chain, using 14 FEB2s is planned for summer 2024.

4. Conclusions

The luminosity upgrade of the LHC requires the development of a new readout chain for the LAr calorimeter at the ATLAS experiment, to meet both TDAQ and radiation requirements. Custom radiation-hard ASICs are designed and tested. With the help of the slice-test FEB2 board, the interplay between the on-detector components was successfully validated. Off-detector ATCA boards with different FPGAs are also available to test and aid firmware development. Integration work has also started to study the interface between on- and off-detector boards. Prototypes for all boards are currently being developed. The project is on track for the HL-LHC.

References

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