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ATLAS Trigger and Data Acquisition Upgrades for the High-Luminosity LHC

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The ATLAS experiment at CERN is constructing an upgraded system for the “High-Luminosity LHC” (HL-LHC), with collisions due to start in 2029. In order to deliver an order of magnitude more data than previous LHC runs, 14 TeV protons will collide with an instantaneous luminosity of up to 7.5×10^{-34} cm^{-2}s^{-1}, resulting in much higher pile-up and data rates than the current experiment was designed to handle. While this is essential to realise the physics programme, it presents a huge challenge for the detector, trigger, data acquisition and computing. The detector upgrades themselves also present new requirements and opportunities for the Trigger and Data Acquisition (TDAQ) system.

The design of the TDAQ upgrade comprises: a hardware-based low-latency real-time Trigger operating at 40 MHz, Data Acquisition, which combines custom readout with commodity hardware and networking to deal with 4.6 TB/s input, and an Event Filter running at 1 MHz, which combines offline-like algorithms on a large commodity compute service with the potential to be augmented by commercial accelerators. Commodity servers and networks are used as far as possible, with custom ATCA boards, high speed links and powerful FPGAs deployed in the low-latency parts of the system. Offline-style clustering and jet-finding in FPGAs, and accelerated track reconstruction are designed to combat pile-up in the Trigger and Event Filter, respectively.

An overview of the planned phase II TDAQ system is provided, followed by a more detailed description of recent progress on the design, technology and construction of the system.

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[*] Speaker

1. ATLAS Phase II TDAQ System

The ATLAS Phase II TDAQ system [1, 2] follows the same general design as the currently existing TDAQ, with four distinct subsystems, each with its own constituents. The overall structure and flow of data and signals is summarised in Figure 1.

1.1 Level 0 Trigger

The **Level 0 Trigger** performs coarse event reconstruction based on low-latency ATCA boards and FPGAs, in order to provide a fast decision on whether to reject the event or to perform more accurate reconstruction at the Event Filter. The rejections reduce the event rate by a factor of 40, from the 40 MHz input to 1 MHz. It comprises five different systems: **L0Calo**, **L0Muon**, **MUCTPI**, **Global Trigger** and **CTP**.

L0Calo handles calorimeter-related reconstruction, based on coarse granularity information. It has several types of Feature Extractors, or FEX: **eFEX** (Electron Feature Extractor, triggers on electrons, photons and taus), **jFEX**(Jet Feature Extractor, triggers on jets and calculates missing transverse energy and other relevant energy sums), **gFEX** (Global Feature Extractor, triggers on large-radius jets, also assists in calculating missing transverse energy and pile-up related corrections) and **fFEX** (Forward Feature Extractor, triggers in the forward region: $|\eta| > 2.5$ for photons and electrons, $|\eta| > 3.2$ for jets).

L0Muon identifies muon candidates. It comprises the **NSW Trigger Processor**, for reconstructing muon tracks using the New Small Wheels, the **MDT Trigger Processor**, which identifies muon candidates in Monitored Drift Tubes, and the **Barrel Sector Logic** and **End-Cap Sector Logic**, which implement both detector control and triggering on signals for these two regions of the detector (covering $|\eta| < 1.05$ and $1.05 < |\eta| < 2.4$, respectively).

MUCTPI, the Muon to Central Trigger Processor Interface, sends muon candidate information to the Central Trigger Processor while avoiding multiple counting of the candidates.

The **Global Trigger** integrates information from L0Calo, L0Muon and higher granularity calorimeter information to reconstruct calorimeter clusters, electrons, photons, taus, jets, missing transverse energy and other topological quantities using offline-like algorithms. Its design relies on a Global Common Module (GCM) that provides the base for implementing the **Data Aggregators** (which use time-multiplexing to aggregate the relevant event information), the **Global Event Processors** (which implement the algorithms to perform the reconstruction) and the **CTP Interface** (which demultiplexes the outputs from the Global Event Processors so that the Central Trigger Processor can use them).

CTP, the Central Trigger Processor, makes the final decision of whether to reject the event or not, based on the output of the other components of the Level 0 Trigger.

1.2 Data Acquisition: Readout and Dataflow

The **Readout** subsystem interfaces with the actual detector to transfer the data to the Dataflow subsystem, also handling detector control, monitoring and configuration. It has two parts: **FELIX** (Front-End LInk eXchange), implemented on a custom PCIe board, which interfaces with the detectors and the commodity network that serves the rest of the DAQ system, and the **Data Handler**, implemented in software that runs on commodity servers, which receives detector data from FELIX via the network and formats it, potentially performing some detector-specific processing.

The **Dataflow** subsystem is broadly responsible for handling the event information once it has been formatted by the Data Handler. It buffers, transports, aggregates and compresses the data, makes it available to the Event Filter and, if the event is accepted, transfers it to permanent storage. It is implemented with commodity servers and commodity storage units, being subdivided in three components: the **Event Builder**, which collects detector information from each detector element and forms an event, the **Storage Handler**, which buffers event data, and the **Event Aggregator**, which prepares event data for permanent storage.

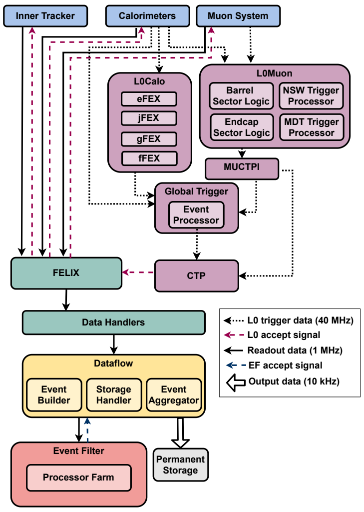

Figure 1: Diagram of the TDAQ Phase II upgrade, showing the four different subsystems: Level 0 Trigger (pink), Readout (green), Dataflow (yellow) and Event Filter (red). Source: [2]

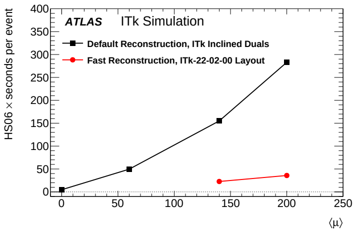

Figure 3: CPU time necessary to reconstruct a $t\bar{t}$ event in the Inner Tracker (ITk) as a function of the average pile-up, for the default and the prototype fast reconstruction software. Source: [2]

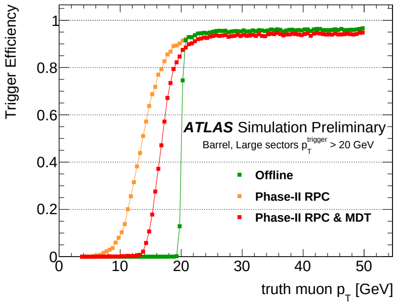

Figure 2: Expected trigger efficiency for L0Muon with (in red) or without (in orange) MDT trigger information, compared to offline efficiency (in green) for a p_T threshold of 20 GeV. Source: [3]

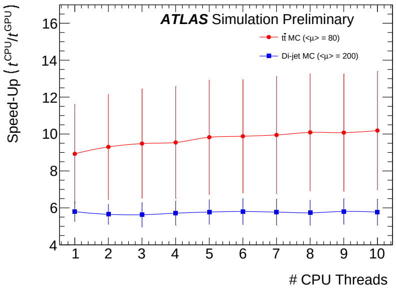

Figure 4: Speed-up of calorimeter topo-clustering from GPU acceleration, for Monte Carlo simulated di-jet and $t\bar{t}$ events, at a pile-up of $\mu = 200$ and $\mu = 60$, for a varying number of CPU threads. Source: [4] Note: This plot is an updated version of the one shown in the poster, from a more recent benchmark of the code.

1.3 Event Filter

The **Event Filter** implements sophisticated reconstruction and classification algorithms, with near offline quality, in order to make a final decision in regards to event acceptance, reducing the 1 MHz input rate by a factor of 100. It is implemented through software running on a farm of commodity processors, with the additional possibility of employing hardware accelerators (such as GPUs or FPGAs) for better throughput and cost and/or energy efficiency. There are three main areas of development when it comes to the event filter, corresponding to the three main sub-detector systems: **EF Tracking**, which depends on the inner tracking detector, **EF Calo**, for calorimeter reconstruction, and **EF Muon**, which, as the name implies, focuses on muon detection.

2. Recent Progress on the Upgrades

2.1 Level 0 Trigger

When it comes to **L0Calo**, the eFEX, jFEX and gFEX will require firmware upgrades, the extent of which is still under assessment, but has been determined to be extensive for eFEX. fFEX, being an addition to the current trigger system, will need to have hardware designed specifically for it, which is currently under development.

For **L0Muon**, the design of a second prototype of a common platform for implementing the Sector Logic is under way, with integration and validation of the firmware also being undertaken. The MDT and NSW Trigger Processors both have prototypes under testing. The simulated effect of the MDT Trigger Processing on trigger efficiency is shown in Figure 2, illustrating that the efficiency with the MDT trigger is improved in comparison to offline reconstruction.

MUCTPI will only need improved firmware to be adequate for Run 4. Requirements and specifications are being collected and some firmware testing is being carried out. For the **Global Trigger**, the third version of the Global Common Module is fully functional and under review. Firmware is being implemented. When it comes to **CTP**, its functionality will be extended, doubling the number of possible triggers in comparison to the current capabilities (from 512 to 1024). Preliminary design and prototyping is ongoing.

2.2 Data Acquisition: Readout and Dataflow

For the **Readout** subsystem, the revision of the second prototype of **FELIX** is finished and the design of a third prototype is in progress. A version of the **Data Handler** was tested with the required 1 MHz Level 0 rate and sub-detector requirements are being collected for further development. Preliminary software for the **Dataflow** subsystem supports the expected data rates, with simulation studies to optimize network and buffer usage under way. Existing and upcoming technologies for network and storage are being actively monitored.

2.3 Event Filter

For **EF Tracking**, one of the major efforts has been integrating with the ACTS (A Common Tracking Software) framework. Use of neural networks for extrapolation in hit pattern recognition and track candidate finding, among other steps, is being explored. The use of GPU acceleration for clustering, seeding and track parameter estimation shows preliminary speed-ups up to a factor of 5 at pile-ups similar to expected run 4 conditions (a pile-up of $\langle\mu\rangle = 200$). FPGA acceleration also looks promising when it comes to Hough transforms, track fitting and neural network based algorithms. Figure 3 exemplifies the improved track reconstruction time with the prototype software available by the time of writing of [2].

For **EF Calo**, a GPU accelerated version of topological clustering [5] is now fully integrated, yielding the same results as the CPU algorithm and showing speed-ups ~ 9 for $t\bar{t}$ events at conditions similar to run 3 ($\langle\mu\rangle = 80$) and ~ 5.5 for di-jet events at conditions similar to run 4 ($\langle\mu\rangle = 200$), as shown in Figure 4, with further optimizations planned. FPGA accelerated cluster making is also under active development, and machine learning based techniques for topological clustering are being explored as well.

Migration to the ACTS framework of track-related code within **EF Muon** is ongoing, in coordination with EF Tracking. Development of machine learning based algorithms for the NSW, with both GPU and FPGA accelerated implementations, is also taking place.

The choice of what kind of hardware acceleration to use, if any, is due for 2025. Given that tracking is the most computationally demanding part of event reconstruction, it will be the major deciding factor.

3. Acknowledgements

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4. References

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