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Performance of Phase-2 CMS Inner Tracker CROC-V1 modules in a serial power chain

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After the end of the Run 3 data taking, the Large Hadron Collider will be upgraded to reach instantaneous luminosities of up to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, allowing the CMS experiment to collect up to $4000\,\mathrm{fb}^{-1}$ integrated luminosity, roughly nine times the amount of data that will have been collected by the end of Run 3. To fully exploit the physics potential of the High-Luminosity LHC, the entire CMS detector will undergo substantial upgrades. The Phase-2 upgrade of the CMS inner tracker aims to build a new tracking detector with higher granularity, longer trigger latency, improved radiation hardness, and extended coverage up to pseudorapidities of $|\eta| = 4.0$. To meet the powering requirements while keeping the material budget low despite a greatly increased number of channels, the Phase-2 inner tracker will implement serial powering of pixel modules. In the TEPX sub-detector, the longest serial power chain will include 11 modules. In this contribution, CMS read-out chip version 1 quad modules will be characterized, with a focus on the comparison between the performance standalone or in a serial power chain.

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1. The Phase-2 Upgrade of the CMS Inner Tracker

The LHC at CERN [1] is the most powerful particle collider ever built. After the end of the Run 3 data taking period, the LHC will be upgraded to reach instantaneous luminosities of up to $7.5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$. The upgrade to the High-Luminosity LHC [2] brings significant challenges for the inner tracking system of the CMS experiment [3]. The average number of proton collision per bunch crossing will increase from 60 to 200, the hit rate in the innermost layer will go up to $3.2\,\mathrm{GHz/cm^2}$, and the amount of radiation increases by a factor of 10 (total integrated dose 1.2 Grad, hadron fluence $2.3 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$). To handle these conditions, while maintaining and even improving on the performance of the current tracker, a completely new tracking detector will be built and installed between 2026 and 2028. The CMS Phase-2 Inner Tracker (IT) features higher granularity, longer trigger latency, and improved radiation hardness compared to the current system and extends coverage up to pseudorapidities of $|\eta| = 4.0$ [4].

The new IT is subdivided into the Tracker Barrel Pixel (TBPX), Tracker Forward Pixel (TFPX) and Tracker Endcap Pixel (TEPX). The pixel modules for the IT contain either 1×2 or 2×2 read-out chips (ROC), developed for CMS and ATLAS by the RD53 Collaboration [5], bump bonded to silicon sensors with a pixel size of $100\times25\,\mu\mathrm{m}^2$. The studies presented in this document have been performed with TEPX quad modules with the second prototype chip, RD53B or CROC-v1 (for CMS Read-Out Chip version 1) [6]. The ROCs are wire-bonded to a High-Density Interconnect (HDI) Printed Circuit Board (PCB) with data readout, bias voltage, and power connection. The four ROCs are powered in parallel, voltage and current sharing is regulated by two shunt-low-dropout (SLDO) regulators for each ROC, powering the analog and digital parts independently.

2. Serial Powering of Pixel Modules

With the increased granularity and coverage of the new IT, powering modules in parallel would require a huge number of cables, significantly increasing the material budget and worsening the physics performance of the new detector. The IT will therefore implement serial powering of pixel modules. In the TEPX sub-detector, the longest serial powering chains will include 11 modules. These have to be electrically insulated from the underlying mechanical structure, as their ground potentials differ within the chain. The applied current has to be high enough to satisfy the highest possible load current in the chain, which comes at the cost of extra power dissipated in the SLDO. As this has never before been implemented for large systems in high energy physics, the performance of the pixel modules in a serial powering chain has to be assessed in detail.

The performance of three digital quad modules (i.e. modules without a silicon sensor) using the CROC-v1 chip is assessed with the modules powered in series and compared to results obtained in standalone operation. A test board has been designed for a first characterization of CROC-v1 modules in serial powering. Data is read out through a Display Port cable connected to the FC7 data acquisition board [7]. The test board is placed in a climate chamber at $-20°$C ambient temperature and the modules are operated at 8 A input current, with analog and digital voltages tuned to 1.2 V. Only eight of the twelve ROCs can be tested reliably: Three ROCs are known from wafer-level testing to only work partially, a fourth has been damaged while handling the module between tests.

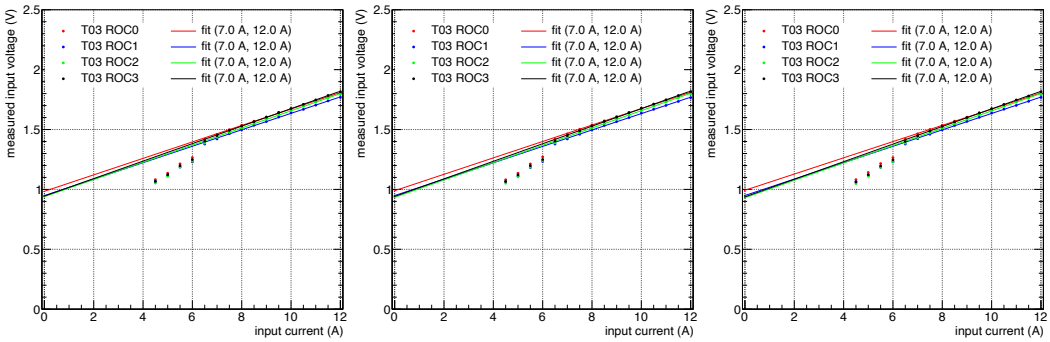

Figure 1: I-V curves of the four chips of module T03; measured standalone (left), in serial powering with the module placed at the beginning of the chain (middle), and at the end of the chain (right).

2.1 I-V curves

The analog and digital input voltage $V_{\text{in,A}}$, $V_{\text{in,D}}$ on each ROC of the module T03 are measured at input currents in the range from 4.5 A to 12.0 A (Fig. 1). Above 6.5 A, the expected linear behavior is observed. A fit to the data points between 7.0 A and 12.0 A yields values for the offset voltage and resistance in good agreement with the expected values of $V_{\text{offset}} = 1.0\,\text{V}$ and $R_{\text{eff}} = 70\,\text{m}\Omega$. No difference between standalone and serial powering is observed.

2.2 Current Overhead

The current overhead is defined as the fraction of the input current that is dissipated at the SLDO, $I_{\text{shunt}}/I_{\text{in}}$, which is measured using the ROC's internal analog-to-digital converter (ADC). The design overhead is around 20%. Figure 2 shows the analog, digital, and total current overhead of each chip on modules T03, T05, and T06. The measurements were performed in standalone and serial-powering mode at the nominal input current $I_{\text{in}} = 8.0\,\text{A}$. No significant difference between standalone and serial powering is observed. The analog overhead of all chips is in the range of 20% to 25%, the digital in the range of 35% to 40%, and the total overhead around 30%, indicating that the modules could be operated at a slightly lower input current than 8.0 A.

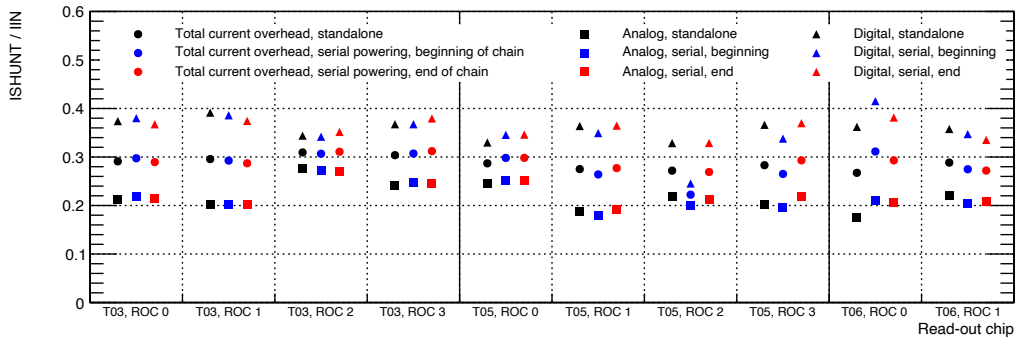

Figure 2: Current overhead of ROCs on different modules. The digital (triangles), analog (squares), and total overhead (circles) are shown. Measurements were performed in standalone (black) and serial-powering mode with the module placed at the beginning (blue) and at the end of the chain (red).

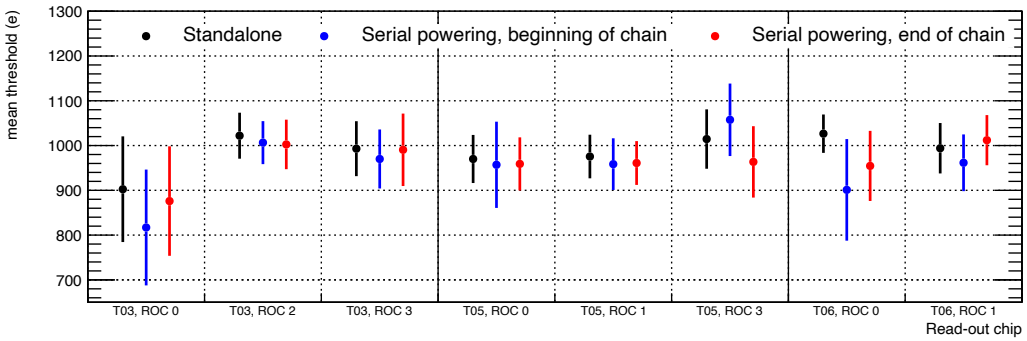

Figure 3: Mean value and standard deviation of the threshold distribution for all pixels in different ROCs. Measurements were performed in standalone (black) and serial-powering mode with the module placed at the beginning (blue) and at the end of the chain (red).

2.3 Threshold and Noise

The chips in all modules are tuned to a threshold of 1000 e^-. An S-Curve is obtained by measuring the hit efficiency while injecting increasing charges through the ROC's internal charge-injection circuit. The threshold is defined as the charge where the hit efficiency reaches 50%. The noise is defined as the difference of the charge value where the hit efficiency is at 30% and 70% respectively. S-Curves are measured for all pixels on each reliably working chip of the three modules. Figure 3 shows the mean value and standard deviation of the distribution of all threshold values measured in standalone and serial powering. For ROC-0 on module T06, the threshold uniformity becomes slightly worse when powered in series. For the other ROCs, no significant difference is observed. Figure 4 shows the mean value and standard deviation for the distribution of the noise values. The noise levels are similar in both configurations for all ROCs.

3. Summary

Three digital CROC-v1 modules were tested in a serial powering chain and their performance compared to standalone operation. No significant differences were observed. More extensive tests using a TEPX disk PCB prototype and optical data readout are currently ongoing.

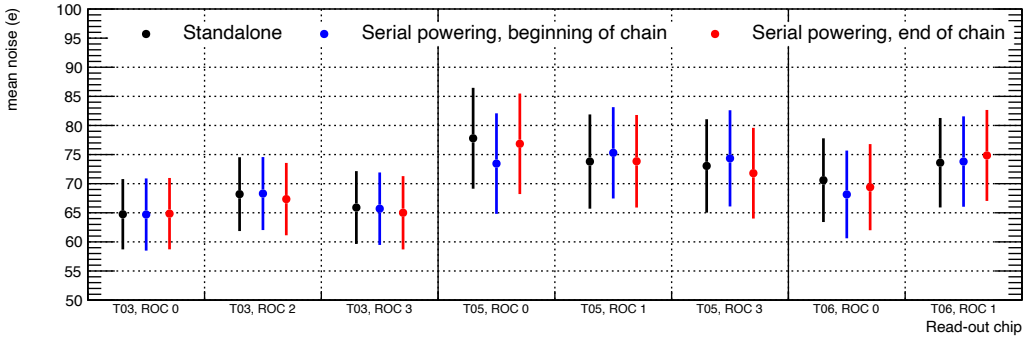

Figure 4: Mean value and standard deviation of the noise distribution for all pixels in different ROCs. Measurements were performed in standalone (black) and serial-powering mode with the module placed at the beginning (blue) and at the end of the chain (red).

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