

The CMS tracker upgrade for the High Luminosity LHC

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The LHC machine is preparing for an upgrade program which will bring the luminosity to about $5-7.5 \times 10^{34}$ Hz cm⁻², to reach an integrated luminosity of 3000–4000 fb⁻¹ over about a decade. This High Luminosity LHC (HL-LHC) scenario, starting in 2029, requires a significant upgrade of the existing CMS detector.

In order to fully exploit the delivered luminosity and to cope with the demanding operating conditions, the whole silicon tracking system will have to be replaced and substantially upgraded before starting the HL-LHC, a plan known as CMS Phase-2 upgrade.

Both the CMS Inner Tracker (IT) detector and the Outer Tracker (OT) will be replaced and the new detector will feature increased radiation hardness, higher granularity and the capability to handle larger data rate. While the IT electronics will handle a longer trigger latency, a key upgrade of the OT detector is to incorporate the identification of charged particle trajectories in the hardware-based (L1) trigger system. A 40 MHz silicon-based track trigger on the scale of the CMS detector has never before been built.

The design choices for the Tracker upgrades are discussed along with some highlights on technological approaches and results from recent prototype testing.

The Eleventh Annual Conference on Large Hadron Collider Physics (LHCP2023) 22-26 May 2023 Belgrade, Serbia

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1. Introduction

An upgraded Large Hadron Collider (HL-LHC) is expected to become operational at CERN from 2029. By increasing its instantaneous luminosity to between 5 and 7.5×10^{34} cm⁻² s⁻¹, the HL-LHC physics program aims at collecting an integrated luminosity between 3000 and 4000 fb⁻¹.

Experiment operation at high-luminosity, however, is challenging. Close to the beamline, radiation damage is very high, with doses up to 12 MGy and fluences up to $2.3 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$. Moreover, the average pileup, i.e. the number of simultaneous proton-proton collisions, averages between 140 and 200, making event reconstruction more difficult.

The CMS experiment is preparing for the HL-LHC. To comply with its new, more demanding operating conditions such as a Level-1 (L1) trigger accept rate of 750 kHz and a L1 latency of 12.5 µs, as well as to survive in a more hostile environment while providing effective means for event reconstruction, the current CMS tracking system shall be replaced by the new Inner and Outer Tracker [1].

2. The Inner Tracker

The innermost region of the CMS detector will host the Inner Tracker (IT), which shall acquire data for precision particle track reconstruction, improving over the current tracking system in granularity, pseudorapidity acceptance ($|\eta| \le 4$) and material budget, while at the same time coping with harsher operating conditions under high luminosity.

The new Inner Tracker is a pixelated hybrid silicon detector. It is built out of modules, arranged onto cylindrical layers in the barrel region (TBPX), and onto double-disc structures in the forward (TFPX) and extended (TEPX) regions (figure 1). Each module incorporates the silicon sensor(s), bump-bonded to 2 or 4 readout chips, as well as the high density interconnect (HDI) for power and signal routing (plus a cooling plate in the TBPX).

IT sensors The silicon sensors all have an active thickness of $150 \,\mu\text{m}$. The standard cell size is $25 \,\mu\text{m} \times 100 \,\mu\text{m}$, a 6-times improvement in the granularity if compared to the current CMS Pixel Tracker. Cells in the sensors are arranged according to a standard rectangular lattice.

Most of the sensors shall be fabricated using n-in-p planar technology. Results from beam tests have shown that these sensors can be operated at high efficiency even after the irradiation expected

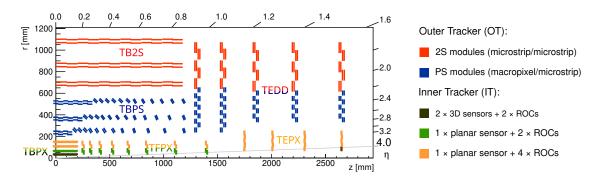


Figure 1: Quarter of cross-section of the CMS Tracker for the HL-LHC.

at HL-LHC [2] for radii greater than 4 cm. Since the innermost layer of the barrel is closer than this to the beamline, usage of planar sensors here is not feasible due to thermal runaway issues after irradiation. 3D sensors will thus be used instead, since they benefit from lower depletion voltage and shorter path length for charge collection compared to planar sensors.

Procurement of the sensors for the Inner Tracker is at an advanced stage, with the orders for production of planar and 3D sensors already placed.

IT readout chip Sensors are read out by the CMS readout chip (CROC) [3], a $2 \text{ cm} \times 2 \text{ cm}$ ASIC developed in 65 nm CMOS technology by the RD53 Collaboration for operation at the HL-LHC. It features radiation tolerance up to 10 MGy, handles hit rates up to $3.5 \text{ GHz} \text{ cm}^{-2}$, and complies with L1 buffering and triggering requirements. The ASIC is a low power device that functions at constant voltage *and* current, which enables its deployment in serial chains using lighter power cables, allowing for a reduced material budget of the system. Sensor charge is processed by the RD53 Linear frontend [4], designed for operation at a threshold of 1000 electrons even after irradiation. Four serial link interfaces are available for high-bandwidth (1.28 Gbps) data output, with conversion to optical at the outer edge of the Inner Tracker, by dedicated "portcards".

The pre-production version of the ASIC, CROCv1, has been available since 2021, while CROCv2 was submitted for production in October 2023.

IT mechanics and services The mechanical structures of the Inner Tracker have purposely been kept relatively simple, so that extraction and insertion of the detector is possible during extended end-of-year shutdowns while keeping the beam pipe in place. This feature will allow the replacement of the innermost TBPX layer and TFPX ring halfway through the High Luminosity program.

Moreover, the system is very lightweight due to the use of carbon foam and carbon fiber for the mechanics, and of evaporative CO_2 cooling, compatible with small (< 2 mm) diameter pipes.

3. The Outer Tracker

The Outer Tracker (OT) is a full-silicon tracking detector, extending radially outside the Inner Tracker. A new feature is the ability to perform online reconstruction of the tracks of charged particles with $p_T > 2 \text{ GeV}/c$, at 40 MHz, so that they can become an input to the L1 trigger system [5]. Such functionality is achieved through the concept of p_T modules.

All p_T modules are assemblies of two segmented sensors, hereafter labeled "top" and "bottom", mutually parallel and separated by a few millimeters. Charged particles with low transverse momenta (p_T) bend more in the 3.8 T magnetic field of CMS, translating to a larger displacement between hits on the top and bottom sensor. By correlating hits on the two sensors, the pairs that are compatible with transverse momenta greater than a set threshold can be selected. These pairs, known as "stubs", are the starting point for online reconstruction of the complete track, which is then used as a L1 trigger primitive.

In the Outer Tracker, p_T modules are either "macropixel-strip" (PS) or "strip-strip" (2S). 2S modules are equipped on both sides with microstrip silicon sensors. Each features two rows of 90 µm × 5 cm strips (totalling a 10 cm × 10 cm active area), which are separately read out by two Front-End Hybrids (FEH). A FEH hosts 8 CMS Binary Chips (CBC) [6] for hit and stub detection, and one Concentrator Integrated Circuit (CIC) [7] for data aggregation. Another hybrid, the Service

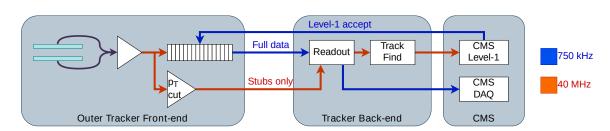


Figure 2: Outer Tracker data path. Stubs are transferred to the back-end at 40 MHz, where tracks are reconstructed and then sent to CMS L1 trigger. Upon its positive decision, the full event data are read out.

Hybrid (SEH), performs DC/DC conversion to power the front end electronics, and interfaces with the backend via optical links (5.12 Gbps uplink).

Operation of 2S modules as p_T modules requires a tight alignment of the strips in the top and bottom sensors, which prohibits the use of a stereo angle to better determine the position of a hit in the direction of the strips. PS modules are thus introduced to improve on this.

In PS modules, the top sensor is again silicon microstrip based ($100 \mu m \times 25 mm$); the bottom silicon sensor is instead segmented into $100 \mu m \times 1.5 mm$ macropixels. Additionally, PS modules have a smaller form factor than 2S modules, with an active area of $5 cm \times 10 cm$. On each FEH, 8 Short Strip ASICs (SSA) [8] per FEH detect hits on the top sensor, and pass them to half of the 16 Macro-Pixels ASICs (MPA) [9] bump-bonded to the bottom sensor, which combine such data with their own hits to form stubs. Data from the MPAs are sent to CICs for aggregation, and then to a Readout Hybrid for transmission to the backend. A Power Hybrid performs the DC/DC conversion.

Like the Inner Tracker, the Outer Tracker consists of barrel and endcap discs. A major difference in the layout is in the barrel, where a tilted geometry is deployed. This more complex arrangement is needed to maximize the p_T modules acceptance for particles from the interaction point.

4. Track finding for the L1 trigger

Stubs from the Outer Tracker are sent to the backend at 40 MHz for track reconstruction (figure 2). This is achieved via custom boards equipped with commercial FPGAs [10].

The trigger system requires the reconstructed tracks to be ready within 5 µs. To comply, the Outer Tracker is split in 9 ϕ -sectors that are processed in parallel; furthermore, each sector is served by 18 boards, so that each board has to process only 1/18 of all events.

Stubs are initially sorted to reduce combinatorics, by taking into account the constraints on the p_T of the track, coming from p_T module operation. Stubs on adjacent layers or discs are then used to seed tracks, that are projected onto other parts of the detector to find all other stubs that are likely to have been generated by the same particle. Here the same track could be seeded multiple times via different stubs, and such redundancy helps against any inefficiencies of the detector modules. In any case, duplicate tracks are merged before refitting with a Kalman filter and checking the quality of the result, which is ready to be forwarded to the trigger system.

The Track Finder algorithm has been tested both at the level of its single steps, and as a chain on real hardware. This allows the ability to check the correctness of the results, as well as measure the latency of the system. As such, developers are able to understand critical aspects of the system, such as the impact of FPGA congestion on timing, and how to approach them.

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