PROCEEDINGS OF SCIENCE

Hybridization and assembly of LGAD devices for the HGTD ATLAS upgrade

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The High Luminosity era will present a challenge in terms of the number of simultaneous interactions (pile-up) to the Large Hadron Collider experiments. In order to mitigate the detrimental effect of the pile-up on physics performance, ATLAS will install a High Granularity Timing Detector (HGTD) that will provide a time resolution per track of 50 ps during its lifetime. HGTD consists of hybrid silicon devices with Low Gain Avalanche Detectors as the sensing medium. The LGADs are segmented into a matrix of 15×15 with 1.3×1.3 mm^2 pads. The sensors are bump-bonded to the readout ASIC (ALTIROC), producing the HGTD hybrid. Two hybrids are joined by a single flexible PCB, defining the HGTD module. In this work, we discuss the hybridization process and its quality control, as well as the studies carried out to ensure that the timing performance of the chip is not affected by the bump-bonding process. This document also presents the assembly procedure, the electrical tests and the thermal cycling studies conducted on the initial module prototypes.

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1. Introduction

The Large hadron collider (LHC) will be upgraded for the high luminosity (HL) phase in the next five years. The HL-LHC aims to achieve high levels of luminosity, with the average number of simultaneous interactions expected to reach 200. This will make particle tracking more difficult due to the proximity of the primary vertices in space. However, their separation in time can be exploited to reduce the effect of pile-up. A novel detector, the High Granularity Timing Detector (HGTD) [1] has been proposed to support the new silicon Inner Tracker (ITk) in the pseudo-rapidity range of $2.4 \leq |\eta| < 4.0$. It enhances the capacity to measure the trajectories of charged particles in both time and space.

Low Gain Avalanche Detectors (LGADs) were selected for their excellent time resolution in the challenging irradiation environments [2] presented by the HL-LHC. The silicon sensors are 1.3×1.3 mm^2 and have an active thickness of 50 μm. Each sensor will be attached to an ASIC using bump bonding. Two of such devices will be joined by a module flex and positioned on opposite ends of a cooling plate. An overlap between the opposite side modules is implemented to ensure that each track records a minimum of two hits on average as it passes through the detector. The design of the ATLAS Timing Read-Out Chip (ALTIROC) prioritises time performance, particularly the timing resolution for a 4 fC charge that corresponds to the charge deposited by a minimum-ionizing particle (MIP) at the end of life.

1.1 HGTD Module

As mentioned above the HGTD module will consist of LGAD sensors with 15×15 pads of a size of 1.3×1.3 mm^2 bump bonded to the final HGTD ASIC with a compatible readout channel array matrix (see figure 1).

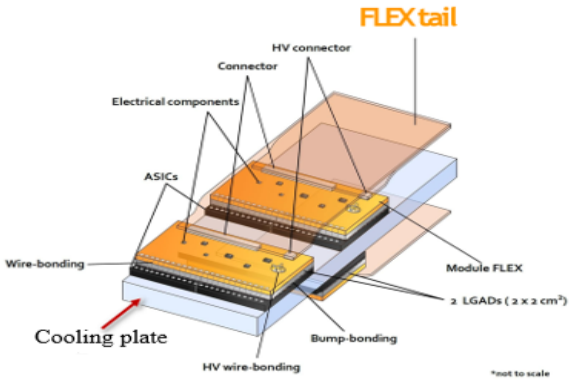

Figure 1: The HGTD module. The figure shows three modules, each consisting of two ASICs bump-bonded to two LGAD sensors, held together with a module flex PCB, that also provides power and allows communication with the ASICs. The flex tail connects the modules to the DAQ system. The modules will be operated at -30 °C. This temperature will be regulated with a CO_2 cooling system.

Two LGAD sensors connected to two readout chips will be combined into a module with a single module flexible PCB (module flex cable), as shown in the figure 1. Through the bump-bonding process, each channel of the sensor is DC-coupled to the corresponding readout channel through a small solder bump ball. This connection between the sensor and readout electronics (also

called hybridization) is a critical step in the HGTD module fabrication, and its yield has to be high to obtain the desired performance of the detector. The module flex is attached to the top of the sensor with glue (Araldite 2011). Properly positioning the basic modules is crucial for achieving the final specifications. Various limitations were considered for optimising the assembly procedure. The overall size of the produced modules must not exceed the dimensions of the mechanical framework they will be loaded into, known as the support unit.

This document outlines the assembly process and shows the performance evaluation of early HGTD module prototypes. Different tests are conducted to confirm that the modules satisfy HGTD requirements and to ensure that the components remain undamaged after assembly. The next part provides a summary of the key elements of the assembly process. Section 3 describes the module readout system and the procedure to determine the device threshold and noise. Sections 4 and 5 will outline the primary results and conclusions of this study.

1.2 Prototype Modules

Three different HGTD module prototypes are used in this work for the studies carried out:

- **Early module prototypes which integrate ALTIROC1 chips with LGAD sensor on a test PCB.** The ALTIROC1 integrates 25 channels organised in a 5×5 grid. These modules are used to study the effect of bump-bond size on the noise level of the modules.
- **The first full scale prototype which integrates LGAD and ALTIROC2 on a test PCB.** The ALTIROC2 is the first full-scale prototype that combines a 225 channels in 15×15 matrix with all the necessary analog and digital functionalities. These modules prototypes were used to study the noise levels in the HGTD ASIC. They were also used to perform the first thermal cycle studies and verify the robustness of the glue (Araldite 2011) according to the HGTD specifications.
- **The first full size HGTD modules that integrates 2 full-size ALTIROC2 modules on a flex PCB.** The module assembly and thermal cycle studies were performed on these modules to verify the HGTD full module specifications.

Further details about the ASICs can be found in [3] and [4].

2. Hybridization and Assembly Process

This section briefly describes the bump-bonding process for connecting the sensor to the ASIC and the assembly procedure of the HGTD module using flex cables.

2.1 Hybridisation

The samples were bump-bonded at IFAE in what is the baseline process for HGTD (as detailed in [5]). The first step of the bumping process consist on the under-bump metalization (UBM) of both sensor and ASIC wafers. These prepares the pads of the dies for the second step, the deposition of the solder bump bonds, which are usually deposited on the ASICs. The third and final step it the flip-chip process, during which the substrates are aligned and thermo-compressed to ensure

the connection of each pad on the ASIC to the corresponding one on the sensor. The result is the hybrid, the connected LGAD sensor with the readout chip.

The prototype LGAD sensors (5×5 pad array and 15×15 pad array) used in these studies were fabricated at HPK and FBK as part of different prototype runs. These sensors included the UBM on the pads. The ALTIROC chips were produced at TSMC and the readout boards (PCBs) were provided by Omega. The UBM of ASICs and sensors was deposited at CNM through an electroless process. The SnAg bumps were deposited through laser jetting at IFAE. The flip-chip process was done at IFAE. After flip-chipping, the devices were reflown with formic acid to improve connectivity. No effort was made during these steps to obtain a given substrate separation. The devices were then assembled, as described below.

2.2 Assembly Process

The HGTD modules have to follow accurate positioning and dimension constraints of the HGTD [1]. This requires a well-organized assembly technique to achieve high accuracy (alignment within 100 μm) and repeatability in the final detector. At IFAE, we used a sequential approach that involves repeating two procedures for each of the two bare modules: (1) applying a glue pattern on the flex side using a customised stamp, and (2) aligning and placing each bare module in its designated position to do the actual gluing. The two procedures are performed using a custom made jigs method, as shown in figure 2.

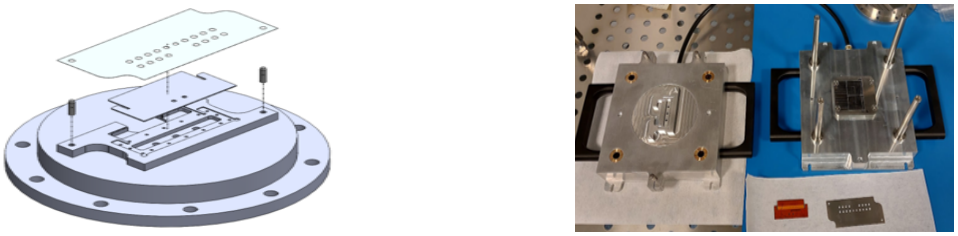

Figure 2: The figure shows the design (left) of the jigs and the actual tools used (left) to perform the module assembly at IFAE.

The area of the module flex beneath the bonding pads must be securely bonded to prevent vibrations while wire bonding. Choosing a stamping process that enables precise selection of the regions to be covered by the glue is essential for meeting the desired requirements. The quantity of the glue applied is measured after each stamping stage which serves as a control parameter. Once the glue (Araldite 2011) is applied to the designated flex area using the glue stamp, each hybrid is positioned in the inlay jig. The upper jig arm with the flex is then placed over the jigs with the hybrids and left for 7 hours for the adhesive to cure.

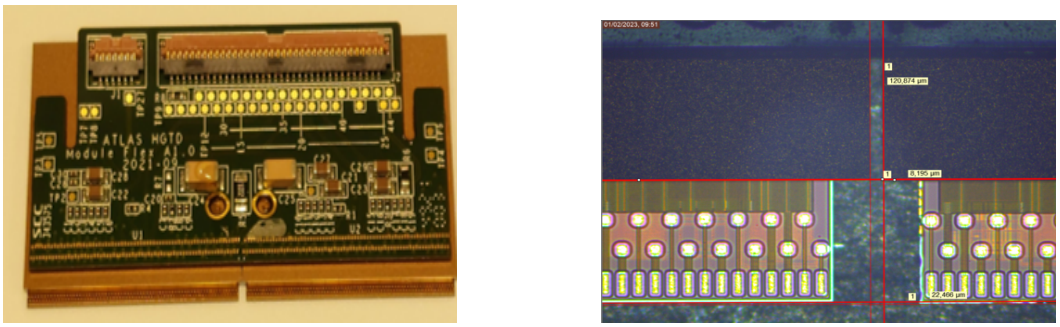

Figure 3: Figure shows full assembled module consisting of two bare modules glued on the flex (left). The meteorology of the module after assembly (right) shows the gap between the bare hybrids, which is ~ 120 μm.

Figure 3 displays the full HGTD module and the meteorology results. Additional dimension limitations, such as the requirement for a minimum spacing of 50 μm between sensors are also met. Both the size and the precise positioning of the hybrids are important for successful wire bonding to the flex, since improper placement could impede or completely halt the wire-bonding process. Therefore, a crucial aspect of the assembly process is the rotation of each module, determined by the spacing between the wire-bonding pads of the ASIC and their flexible counterparts, measured at the edges of each chip. Although the requirements do not specify a maximum rotation value, rotations above ± 0.1° are believed to potentially disrupt the wire bonding process. The rotation measured for the module was measured to be below 0.075°. Figure 4 shows a detail of the wires after of a module. The wire bonding is done from wedge to wedge. Pull tests were also performed for the quality assurance as shown in figure 5.

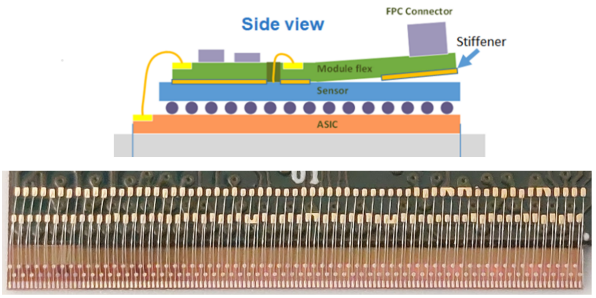

Figure 4: The figure displays the module schematics with the wire bonding and the module wire-bonding done wedge to wedge

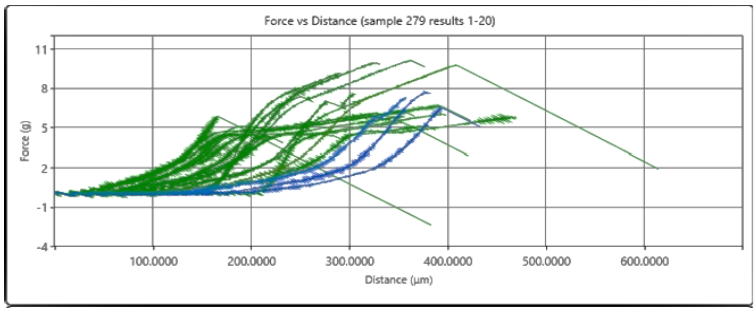

Figure 5: Pull test results of the module wire-bonding. All the wires satisfy the 5 gf requirement of HGTD [6].

2.3 Available Devices

Table 1 lists the devices under test that were assembled for the measurements performed in this work. These are referenced in the following sections of this paper.

DUT name	ASIC	Size	Sensor	Mounted on
Module1-X1	ALTIROC1	5×5 channels	HPK	PCB
Module2-X3	ALTIROC1	5×5 channels	HPK	PCB
Module3-X1	ALTIROC1	5×5 channels	HPK	PCB
B10	ALTIROC2	15×15	HPK	PCB
B207	ALTIROC2	15×15	HPK	PCB
M002	ALTIROC2	$2 \times (15 \times 15)$	FBK	Flex PCB

Table 1: The table shows the list of the devices used to perform the studies as mentioned in section 1.2. HPK and FBK correspond to the sensor fabrication sites, Hamamatsu Photonics and Fondazione Bruno Kessler, respectively.

3. Module Testing

The setups for the measurements with ALTIROC1 and ALTIROC2 module prototypes are shown in figure 6. It consists of test boards (PCBs) where the ALTIROC devices were mounted and connected to a FPGA board (interface board and then to the FPGA in case of the ALTIROC2 devices) using a PCIe cable in case of the ALTIROC1 devices and Samtec cable in case of the ALTIROC2 devices. A similar setup was used for the ALTIROC2 module using the module flex.

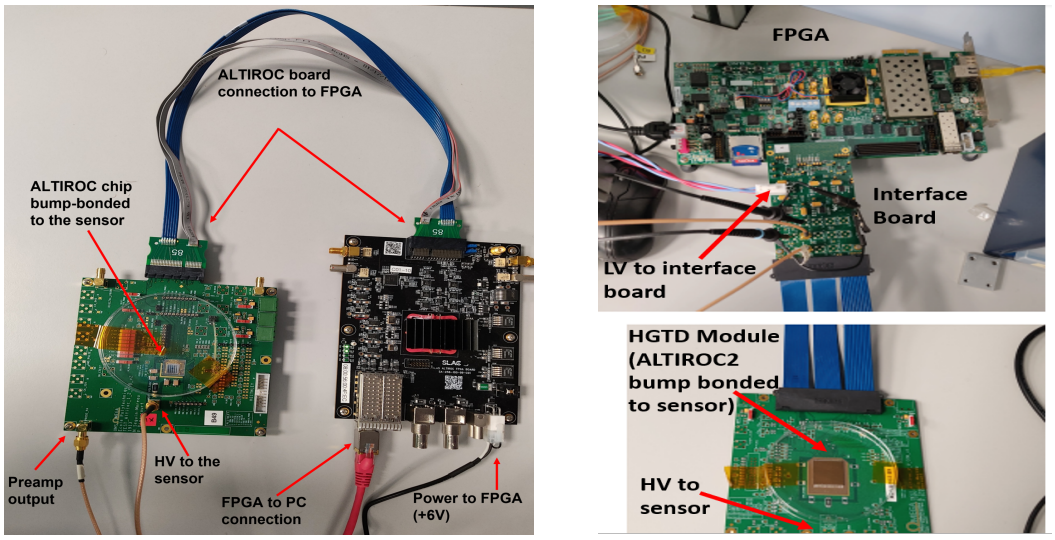

Figure 6: ALTIROC1 module (left) and ALTIROC2 module (right) test bench setup

The ALTIROC1 and ALTIROC2 chips include the charge injection mechanism that allows to inject charge in each pad of the chip, simulating the signal of the incoming particles. A calibrated charge is injected through the injection capacitor (C_{test}=200 fF), which can be controlled through the slow control parameters. This pulse is delivered at the pre-amplifier input. After the signal is amplified, the pre-amplifier output goes to the discriminator, which uses a programmable threshold set by a DAC 10-bit register. Finally, the discriminator output gives the information of timing and number of hits received through the Time-to-Digital Converters (TDCs) and a hit-flag.

3.1 Readout System

Different readout systems were developed to characterise the HGTD modules. In this work atlas-altiroc-daq software (developed in France, which was later improved and named FADA to test the new version of the chip) is used to perform the noise study with ALTIROC1 modules. Alvin is used to investigate the ALTIROC2 modules in this study. Alvin is a data acquisition (DAQ) system developed at IFAE for the retrieval of data from the ATLTIROC2 chips and later versions. This system enables us to control the front-end chips. It can set DACs for threshold setting and control the chip injection mechanism. The noise can be determined from the S-curves obtained as explained in the next section. By using a set of procedures known as "scans," several aspects of the pixel's performance are examined. In the case of "source scan", charge is not injected as the chip detects the intrinsic charge produced in the sensor pixels with an external source.

3.2 Module noise determination procedure

The "threshold scan" procedure in Alvin is used for evaluating the noise characteristics of the individual pixels. In this scan, a signal is injected through the internal capacitor, with a very precise injected charge at the preamplifier input. To register a signal as a particle hit, the voltage measured must surpass a specific threshold value. If a pulse falls below the threshold, it will not be recorded by the acquisition system. This fixed charge is injected into the pre-amplifier at a fixed value of the threshold (DAC-bit threshold). This charge injection is repeated multiple times and the percentage

of the injections that result in a hit being readout is recorded. The hit efficiency is thus defined as the percentage of the number of hits registered to the number of hits injected. The value of the injected charge is then increased by a voltage step and the process is repeated until a specific charge range has been covered. The charge range of 0 - 25 fC was used in this work (in case of the tests with Alvin). This threshold scan should produce a step function, with none of the injections resulting into a hit for any charge value below the threshold and all the injections resulting into hits for any charge value above the threshold.

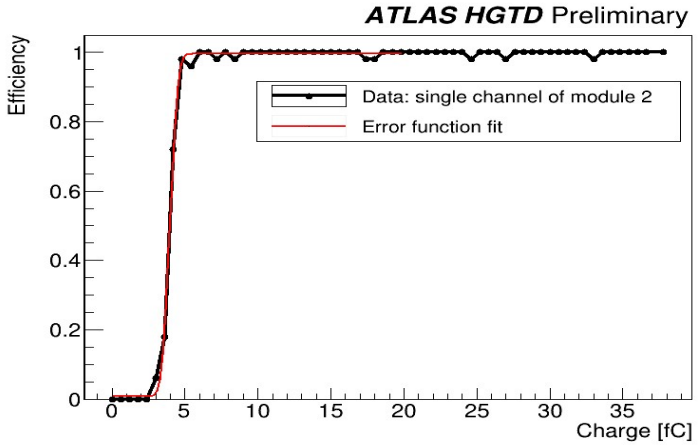

Figure 7: An example of the S-curve fit, corresponding to the efficiency as a function of the injected charge for a single channel of module 2 mentioned in the table 1.

Nevertheless, due to the electronic noise of each channel, this step function is spread into an S-curve shape as shown in figure 7. The S-curve is fitted with a Gaussian error function:

$$d + \frac{c \times (1 - Erf\frac{(x-a)}{\sqrt{2}b})}{2} \tag{1}$$

where the mean value, a, of this fit is defined as the threshold for each channel and the σ of the fit, b, is defined to be the noise for each channel.

3.3 Bump-connectivity Determination

The "source scan" in Alvin is used to examine the bump connection in the modules. The procedure involves using a radioactive source, namely a Sr-90 beta source, to generate signals in the sensor pads, which are then processed by the readout chip. This test enables the verification of the complete bump-bond connectivity of the module.

4. Results

4.1 Effect of Bump-bond on Noise

The noise and the gain of the readout channel is effected by the sensor capacitance. However, bump bonds can also affect the input capacitance seen by the pre-amplifier. Furthermore, the separation between the chip and the sensor could affect the noise of the device through coupling between the

substrates. In order to understand the impact on the noise of the HGTD modules generated by bump-bonding effects, noise differences were studied in ALTIROC1 module hybrids with standard solder balls (80 µm diameter), called X1 and hybrids with solder balls three times as big (115 µm diameter), called X3.

If bump-bonding parameters like ball size and substrate separation affect the performance of the modules, the effect will be apparent when comparing the noise levels in these devices. The noise for each channel of each board is shown in figure 8 with and without the bias voltage applied to the sensor.

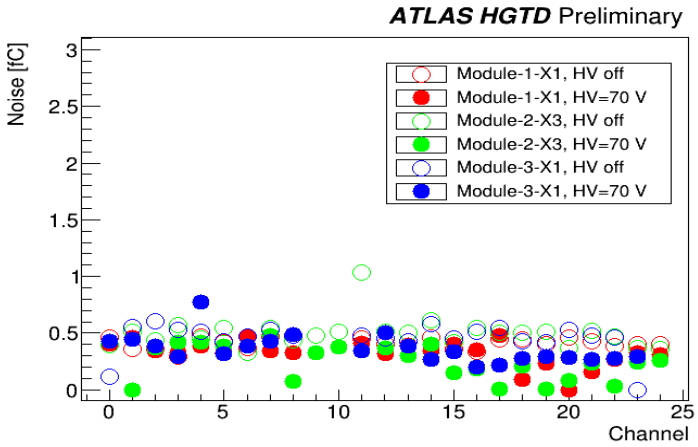

Figure 8: Noise of all channels of the three tested boards obtained from the S-curve fit with and without HV at room temperature.

The noise is expected to be lower when the High Voltage (HV) is applied as, with an increase in HV, the depletion depth of the sensor increases, decreasing the sensor capacitance. As the sensor capacitance is directly proportional to the noise, a lower noise is obtained after applying the HV to the sensor. In the results shown above, lower noise is observed when HV is applied (Solid circles) in comparison to the noise when no HV is applied (empty circles). Moreover, the results of these noise measurements for the three tested boards don't show any significant difference betwen X1 and X3 devices. The bump size of about 80 μm was selected to bump bond rest of the devices after these tests.

4.2 Minimum Detectable Charge

As the sensor performance will decline with irradiation, the ASIC should be able to set a threshold for small input charges. A minimum threshold of 2 fC is decided for the ALTIROC which should yield a hit efficiency above 95% for a 4 fC input charge.

Figure 9 shows the S-curves obtained from the threshold scans in Alvin in the ALTIROC2 device B10 at a target threshold of 6 fC and 3.2 fC.

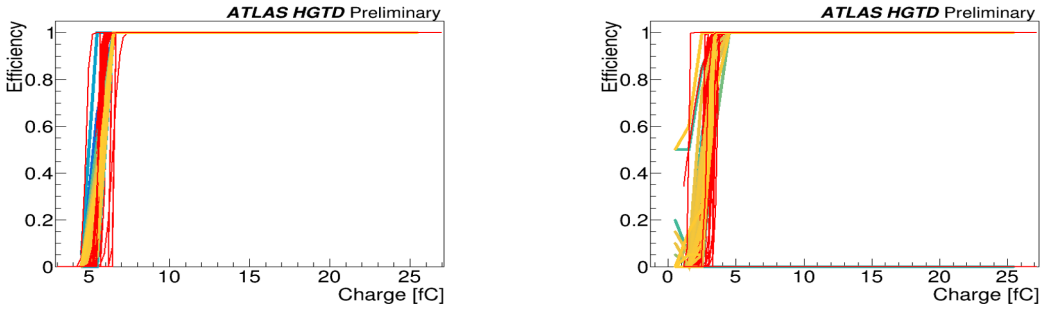

Figure 9: S-curves obtained from the threshold scans in B10 are shown at a target of 6 fC (left) and 3.2 fC (right). The measurements were done at room temperature and module was biased at 90 V.

The noise at a target threshold of 3.2 fC is obtained to be ≈ 0.3 fC. A minimum detectable charge of 3.2 fC is achieved in this work, which meets the HGTD requirements. The minimum detectable charge in ALTIROC2 modules is 2.9 fC, as reported in [4]. These results are consistent with the studies of the other ALTIROC2 devices.

4.3 Bump Connectivity Studies

As mentioned in section 1.1, the HGTD modules will be operated at $-30\,°C$. The modules undergo thermal stress as a result of the temperature variations during its lifetime. This will produce stress on the bump bonds due to the different coefficient of thermal expansion (CTE) between module components, which may damage the bump connections. It is expected that the differences in the CTE between the different materials will be small enough that sudden changes in temperature will not cause any mechanical damage. In order to test the mechanical robustness, the modules will be put through thermal cycles that simulate the extreme operating conditions between −45 °C and +40 °C.

Initially, the effect of glue alone on the bump bond connectivity due to the thermal effects is studied. Figure 10 shows the source scan after thermal cycle on the ALTIROC2 module with only glue on the top of the module. Note that in the ALTIROC2 ASIC there is no bump- bonding pad in the bottom left pixel (0,0), which is instead routed to the periphery of the ASIC to study the analog output signal directly.

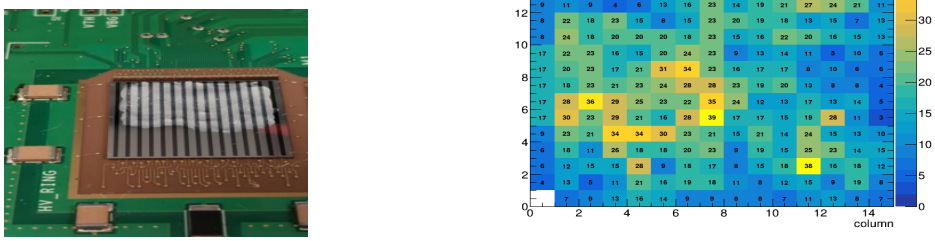

Figure 10: B207 is shown with only glue on the top (left). The source scan (right) after 28 thermal cycle in the range of −45 °C to +40 °C is also shown. The module is biased at 100 V.

It can be seen that the bumps are connected after 28 thermal cycles in the range of −45 °C to +40 °C, showing the stability of the glue in the extended temperature range. Bump connectivity studies were then conducted on the first full scale flex HGTD module, as shown in figure 11.

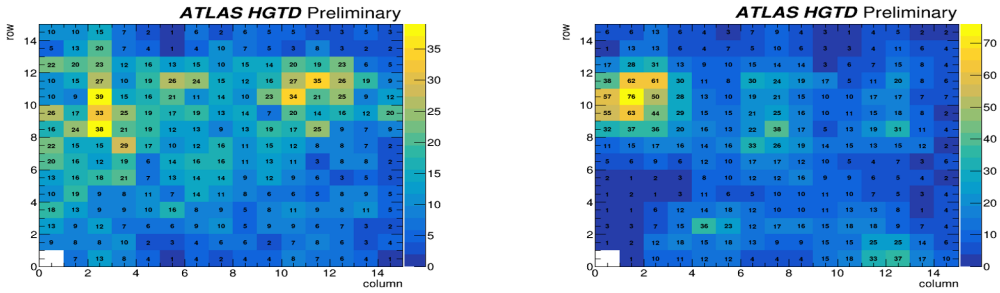

Figure 11: Source scan result at room temperature for the module M002 assembled at IFAE are shown for chip 0 (left) and chip 1 (right) before thermal cycle. The module is biased at 150 V.

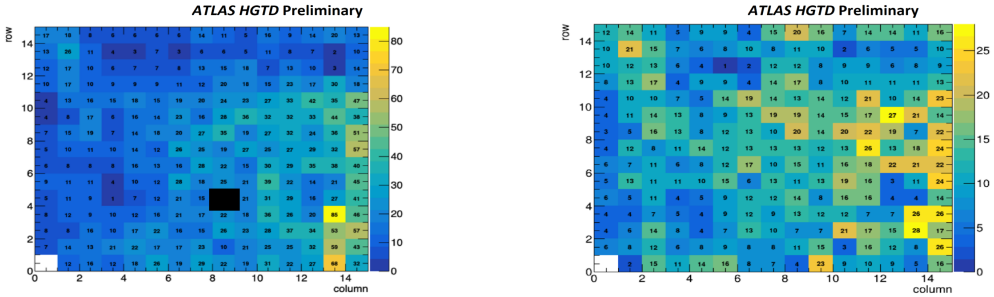

Figure 12: Source scan result at room temperature for the module assembled at Institute for high energy physics (IHEP) is shown for the chip 0 (left) and chip 1 (right) before thermal cycle. The module is biased at 150 V.

It can be seen that the bumps are connected after the assembly in both the HGTD assembly sites (IFAE and IHEP) showing a successful HGTD assembly procedure. The IFAE module (M002) then underwent 68 thermal cycles in the range of from −30 °C to +40 °C. Figure 13 shows the occupancy map obtained from the source scan after the thermal cycles.

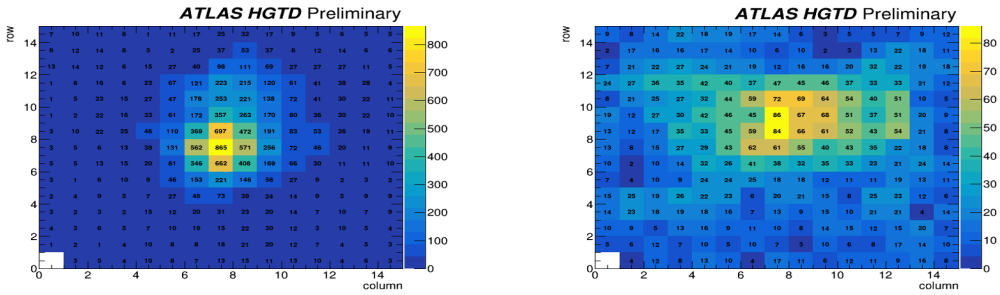

Figure 13: Source scan result at room temperature is shown for module M002 is shown for chip 0 (left) and chip 1 (right) after the 28 thermal cycles in the range of −30 °C to +40 °C. The module is biased at 150 V.

It is observed that the module keeps the bump connectivity in the range of −30 °C to +40 °C after total 68 thermal cycles. Further studies are being performed in the extended temperature range.

5. Conclusions

ATLAS plans to install a new High Granularity Timing Detector to reduce the impact of pile-up during Run 4. HGTD will include 8032 modules which will consist of LGAD sensors with a pattern of 15×15 pads bump-bonded to the corresponding readout chips. An initial smaller (5×5) version of the hybrids prototypes were produced to evaluate the effect of the bump-bond size on the device performance. Using the atlas-altiroc-daq readout system it was found that increasing the size of the bump bond by a factor of three does not effect the noise level of the module. Full size ALTIROC2 prototypes were also assembled and evaluated. In the studies presented in this work, the main objective was to check the communication with the readout chips and verify the connectivity of the devices using another readout system developed to this end (Alvin). The threshold of the readout chips was adjusted to be able to operate the devices to detect passing-through particles. Using an external radiation source we analysed the connection between the front-end ASIC and the sensor to confirm that the modules were undamaged during assembly and that all the channels in the devices were working. It was also verified that the connections are not damaged after the thermal cycles of the modules in the temperature range of −30 °C to +40 °C. The modules were shipped to LPNHE (Paris) for further loading tests. Further studies are conducted in the extended range with full HGTD prototypes with ALTIROC3 and pre-production sensors showing promising results. Different HGTD institutes are now building the necessary tools and processes to prepare for the upcoming pre-production stage expected to be completed by the beginning of 2025.

6. Acknowledgments

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