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ITS3: the next upgrade of the ALICE Inner Tracking System

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The ALICE experiment, optimized to study nuclei collisions at the ultra relativistic energies provided by the LHC, is approaching to a new upgrade phase, foreseen in 2026 during the third Long Shutdown of the accelerator. This upgrade includes the replacement of the 3 innermost layers of the Inner Tracking System, the detector closest to the interaction point, which is currently made of 7 layers of Monolithic Active Pixels Sensors (MAPS). The main features of this new vertex detector, named ITS3 are the extremely low material budget (only 0.07% X_0 per layer) and the reduced radial distance of 19 mm to the interaction point. To achieve this goal, the ITS3 will be made of wafer scale MAPS, thinned down to 50 µm and curved in order to ensure a true cylindrical geometry, without any flexible printed circuits in the active area. The mechanical support and the cooling system will be optimized to reduce the total material budget: the layers will be kept in place thanks to ultra-light carbon-foam support elements, and they will be cooled through a speed air flow.

The success of the project depends on many interconnected aspects and an intense R&D activity is ongoing to investigate all technological aspects related to the development of the sensor, mechanics, cooling, and integration. This paper summarizes the status of the project and presents selected results from the characterisation of the first prototype chips.

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1. Introduction and upgrade motivations

ALICE (A Large Ion Collider Experiment) [1] is the LHC (Large Hadron Collider) experiment especially designed to study the physics of strongly interacting matter at extreme energy densities, where a phase of matter called quark–gluon plasma forms. After 10 years of data taking, during the LHC Long Shutdown 2 from 2019 to 2021, ALICE underwent major upgrades to improve its tracking and readout capabilities [2]. One of the key components of these upgrades is the new Inner Tracking System (ITS2), which is the largest pixel detector built to date, as well as the first silicon tracker with monolithic active pixel sensors (MAPS) at the LHC. It consists of 7 layers of ALICE PIxel DEtectors (ALPIDEs) chips [3] with 27×29 μm^2 pixels, for a total of 12.5 Gigapixels covering 10 m^2 of active area. The material budget of only 0.36% X_0 for each of the 3 innermost layers, and 1.1% X_0 for each of the 4 outermost ones, ensures excellent tracking precision and efficiency, especially at low transverse momentum.
The ITS2 is successfully taking data since the beginning of LHC Run 3 in July 2022, showing excellent performance during both proton–proton and Pb–Pb collision data-taking periods. A further upgrade to the ITS2, called ITS3 [4, 5], is foreseen in the next years, with the main aim of placing the innermost layer even closer to the interaction point. Hence, the Inner Barrel, i.e. the 3 innermost layers, will be replaced with a new ultra-light detector. The design of the ITS3 suppresses all extra material that is not actively used for particle detection and tracking. This will result in a further improvement in the detector's pointing resolution and tracking efficiency, which will be crucial for ALICE operation in the Run 4.

2. The ITS3 detector

Some really innovative features characterize the ITS3 project. Firstly, the 3 layers of the ITS3 are made of wafer-scale sensor ASICs, where each half-layer is constructed as a single piece of silicon. The fabrication of large area sensors is feasible thanks to the stitching technique, which allows us to exceed the typical field of view of the lithographic equipment and connect several identical design units without any external circuit boards. Only 6 sensors are thus needed to assembly the ITS3 detector, as illustrated in Figure 1. Since the sensors will be thinned down to ~50 μm, they can be bent to the target radii of 19.0 mm, 25.2 mm, and 31.5 mm, reproducing a truly cylindrical geometry. The widths of the 6 sensors are 56 mm, 75 mm, and 94 mm for layer 0 to layer 2, respectively, while the length in the beam direction z is the same for all layers – 266 mm.

Another impressive feature of the ITS3 detector is its extremely low material budget, which will be reduced to 0.07% X_0 per layer. This result is achieved by removing all the "unnecessary" material in the current ALICE inner tracking system, by eliminating water cooling, flexible printed circuits (FPCs) carrying power and data signals, and most of the support structures in sensitive areas. Air cooling instead of water cooling has been proven to be compatible with the sensor power consumption of 40 mW/cm^2. The external FPCs can be removed by integrating the data and control signals and power distribution on the sensor silicon. Finally, the bending of large area sensors ensures a self-supporting arched structure requiring only light mechanical supports made of carbon foam.

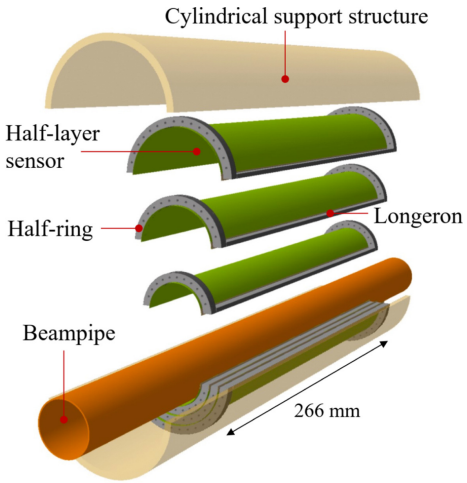

Figure 1: Schematic layout of the ITS3. The 6 stitched, wafer-scale pixel sensors are depicted in green [4].

3. Selected results on R&D activity

The challenging requirements described in Section 2 call for an intense R&D activity, the main results of which are described below.

3.1 Sensor bending

The bending procedure was tested under several conditions and for different radii. Several tests were performed at Desy and SPS in 2020-2021, where ALPIDE chips thinned down to 50 µm and bent to the ITS3 radii were characterized under beam. It has been shown that the detection efficiency and spatial resolution are consistent with flat ALPIDEs. Inefficiency remains below 10^{-2} in a wide charge-threshold range, notably achieving values of 10^{-4} at the typical operating point of approximately 100 electrons [6]. The tests continued on small test structures (MLR1) produced for the ITS3 in 65 nm CMOS technology and results show that no degradation because of sensor bending is observed.

3.2 Air cooling and thermo-mechanical characterization

To ensure acceptable levels of thermal noise, the air cooling system has to be designed to keep the operational temperature of the sensor below 30 °C across the sensor surface, with a maximum gradient of 5 °C. Moreover, the material selected to keep the bent sensors and the FPCs to their nominal position has to introduce a minimum amount of material budget and, in addition, ensure an efficient dissipation of the heat produced by the sensors. For this reason, the Carbon Duocel foam has been selected for the fabrication of ultra-light supports thanks to its low density (45 kg/m^3) but high stiffness, whereas the Allcomp K9 standard density RVC foam, characterized by high thermal conductivity (25 W/(m K)), has been selected for cooling radiator.
Several breadboard models have been assembled and tested inside a custom wind-tunnel in order to study both the heat dissipation and the mechanical stability. When experimentally reproducing the expected power consumption of the sensors, i.e. roughly 40 mW cm^{-2}, a free-stream airflow of 20 °C at an average velocity of 8 m s^{-1} is sufficient to meet the ITS3 requirements and keep the sensor

at the nominal operating temperature of 25 °C, in good agreement with the computational fluid dynamics simulations [5]. Under the same experimental conditions, vibration measurements show that the amplitude of displacement has RMS smaller than 0.4 µm and the maximum displacement is about 1.1 µm.

3.3 Technology validation

Unlike the ALPIDEs, which were produced in a 180 nm CMOS imaging process provided by TowerJazz, the sensors for the ITS3 will be fabricated in the 65 nm technology, which will be employed for the first time in a such kind of application, allowing for a denser design of the chip and for production on larger wafers (300 mm vs 200 mm). To validate this technology, an intense R&D activity was performed on many small analog and digital test structures from a first prototype run on a multi-layer reticle (MLR1). Several pixel variants, which differed by doping levels, pixel geometries, and pixel pitches, were tested both in laboratory and in beam tests. The main goal was to verify the radiation hardness and the detection efficiency of the MAPS produced in this technology. Figure 2 shows the effect of different irradiation levels on the detection efficiency and the fake-hit rate for a digital pixel test structure. As expected, the non-ionising radiation mostly degrades the charge collection efficiency, whereas the largest effect of ionising radiation damage is on the noise (front-end) performance. At a radiation load of 10^{13} 1 MeV n_{eq} cm^{-2} (NIEL) and 10 kGy (TID), corresponding to the ITS3 radiation hardness requirement, a detection efficiency above 99% was reached while preserving the fake-hit rate below 0.01 $pixel^{-1}$ s^{-1}. These results were obtained at room temperature (20 °C).

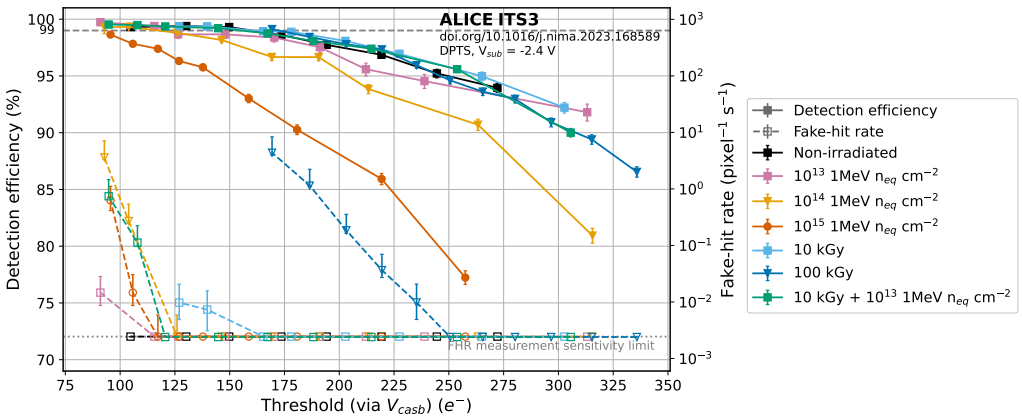

Figure 2: Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of average threshold, for different irradiation doses indicated by colour (see Ref. [5, 7] for more details).

The spatial resolution performance was also evaluated for different pixel variants and no degradation related to the received dose was observed: the spatial resolution measured is equal to or even slightly better than that of a purely binary sensor (pixel pitch divided by $\sqrt{12}$). Finally, the average cluster size slightly decreases with the increasing non-ionising radiation dose, probably as a consequence of the deteriorated charge-collection process. More detailed results on the characterization of small test structures can be found in Refs. [5, 7, 8].

3.4 Stitching

The first sensor submission, MLR1, was followed by the engineering run 1 (ER1) dedicated to the qualification of stitching in the 65 nm process and estimate of the production yield. This step is crucial for the production of wafer-scale sensors, where repeated sensor units (RSU) are placed next to each other on the wafer and interconnected by stitching during the processing of the silicon, to ensure data transmission and power distribution over the full area of the sensor.
Two large stitched sensors, the monolithic stitched sensor (MOSS) and the monolithic stitched sensor with timing (MOST) have been fabricated and are now being extensively characterized. MOSS is the largest of the two chips, measuring about 259 mm × 14 mm. It is made by ten RSUs stitched together plus two smaller end-cap regions on the sides. Each RSU contains a top and a bottom half-unit, each divided into four pixel regions. The top and bottom half units have a slight design variation in pixel size. All stitched units can be connected and operated independently and be powered down in case of defects. MOSS sensors were firstly tested on wafers with a probe card before thinning, and on wire bonded chips, in the lab and under beam, verifying all basic functionalities and performance. Even if the characterization is still ongoing, the first results show the chip to be functional and fully efficient, confirming the feasibility of using wafer-scale chips for particle detection. Figure 3 shows some preliminary results on MOSS chip performance during a test beam at the CERN PS: at an optimal working point, one of the regions of the MOSS chip achieves a detection efficiency above 99% with a fake-hit rate below 10^{-6} pixel^{-1} event^{-1} [5].

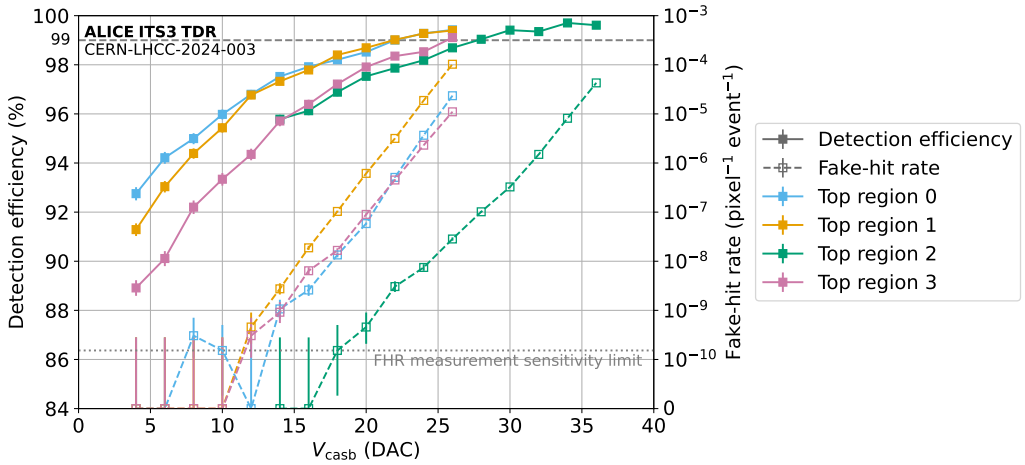

Figure 3: Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of V_{casb} (inversely proportional to the charge threshold) measured with MOSS at the CERN PS (see Ref. [5] for more details).

4. Outlook

This R&D activity provided important inputs for the design of the fully functional ITS3 sensor prototype, the MOSAIX, which will be submitted to the foundry in fall 2024 (ER2). MOSAIX will be composed of RSUs, each splitted in identical tiles, for a total of 144 tiles. Each tile can be thought of as an independent sensor, which can be independently powered, controlled, and read

out. The design of MOSAIX will be optimized in order to mitigate local defects on the basis of the defect densities observed in ER1. Finally, the last engineering run (ER3) is scheduled for 2025 for the production of the ITS3 final sensors, in order to be ready for the detector installation expected between 2026 and 2028.

5. Conclusions

The new three innermost layers of the ALICE Inner Tracking System (ITS3) will be installed for LHC Run 4. The technology envisaged for this upgrade is based on the use of wafer-scale, bent sensors produced using the stitching technique. All components, from the sensors to the mechanics and air cooling system, are designed to reduce the material budget to unprecedented levels. Several key objectives have been already achieved: silicon sensors with a thickness of 50 µm can be bent to radius tighter than the target 19 mm before breaking, preserving the detection performance; the 65 nm CMOS technology was validated, achieving the detection efficiency > 99% and fake-hit rate < 0.01 pixel^{-1} s^{-1} at the irradiation levels expected for the ITS3; finally the stitching technique was successfully demonstrated by testing the first prototypes of stitched sensors.

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