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ALICE Inner Tracking System upgrade, ITS3: characterization of first chips fabricated in 65 nm CMOS technology

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The Inner Tracking System of ALICE (A Large Ion Collider Experiment) will undergo a major upgrade during the next Long Shutdown of the LHC aimed at enhancing the tracking capability [1]. In particular, the three innermost sectors of the current vertex tracker will be replaced by truly cylindrical layers produced by using curved (wafer-scale) silicon sensors thinner than 50 μm, based on monolithic active pixel structures realised in a 65 nm CMOS process. The innermost layer will be placed at only 19 mm of radial distance from the interaction point [2] guaranteeing at the same time a material budget as low as 0.09% of a radiation length X_0 [2]. The R&D on the sensor ASICs involves a series of submissions in silicon and the first one (named MLR1: Multi-Layer per Reticle 1) was completed at the end of 2020. MLR1 provided several test structures containing transistors, memories and small matrices of pixels with integration of front-end electronics inside the sensitive area of the pixels; these devices have been used to qualify the technology in terms of performance and radiation hardness. In particular, to evaluate the charged particle detection performance, this first submission includes 3 variants of pixel matrices: analog pixel test structure (APTS, 4x4 pixels of 10, 15, 20 and 25 μm pitch, with analog readout); digital pixel test structure (DPTS, 32x32 pixels of 15 μm pitch, with digital in-pixel discrimination and digital readout); CE65 (64x32 pixels of 15 μm pitch and 48x32 pixels of 25 μm pitch, test structures with rolling shutter analog readout). This contribution will provide an overview of these test structures, describing the results of characterisations performed with radioactive sources and beam tests in order to choose the best trade-off between pixel pitch and sensor configuration, optimising charge collection efficiency and stability after radiation damage. The obtained results show a satisfactory behaviour as 99% efficiency for minimum ionising particles and charge collection time resolutions of few ns, giving the direction for the next submission (ER1: Engineering Run 1) directed to large, stitched sensor chips.

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1. Introduction

ALICE (A Large Ion Collider Experiment) is the experiment installed along the Large Hadron Collider (LHC) dedicated to heavy-ion physics. Inner Tracking System (ITS) is the innermost subdetector of ALICE and is used to reconstruct primary and secondary vertexes of the reaction. During the study of particular physics processes, such as the decay of short-lived heavy hadrons or resonances in the dielectron channel, it has been found the necessity to improve the detector in order to obtain a better separation of interaction vertexes and a reduction of electron background, so the necessity to improve the tracking resolution and reduce the material budget of the apparatus. For these reasons the ALICE collaboration scheduled an upgrade [1] that is based on replacement of the 3 innermost layers of the existing tracker with cylindrical sensors [3].

The upgrade is based on the technology of MAPS, already used for the existing tracker. Among the advantages of this technology, we have the inclusion of detector and readout electronics in a single chip (then the elimination of hybrid structures) and a low capacitance of the diode obtained through a small collection electrode, that allow the desired reduction of power consumption. But for the new tracker the stitching process and the bending of the final (large area) sensors require the thinning of the device below 50 μm so for the ITS3 the technology node has been reduced from 180 to 65 nm.

2. MLR1: First chip submission in 65nm CMOS imaging process

The first test structures of the project have been realized at the end of 2020 for the qualification of the technology at 65 nm. This first submission, called MLR1, provided 55 prototype chips that have been used to study the behaviour of these structures after the reduction of the technology node, with particular regard to charge collection and radiation hardness.

For the sensor optimization, 3 different types of pixel have been realized (following the experience gained at 180 nm during the previous upgrade of ITS [4]): the *standard* type, that is characterized by a spherical depleted region; the *modified*, in which the depletion region has been extended up to the edge of the pixel; the *modified with gap* were the depleted region has been shaped introducing a gap near the edge of the pixel in order to increase the component of electric field directed towards the collection electrode [5].

Moreover, in order to improve the depletion of the diode and the isolation between the readout electronics and the sensor, 4 different splits have been performed for subsequent adjustment of deep positive and negative wells. All these modifications provided an important improvement in terms of charge collection efficiency, radiation hardness and suppression of charge sharing.

The main prototypes produced are classified in three categories. The first is the APTS (Analog Pixel Test Structure) [6], that consists of chips with 6×6 pixels (only central 4×4 read out) and pitch of 10, 15, 20 and 25 μm; they are equipped with 2 versions of output buffer and are used for the study of the different pixel designs. The second category includes the DPTS (Digital Pixel Test Structure) [7], that consists of chips with 32×32 pixels and pitch of 15 μm; these chips are equipped with an in-pixel full-digital front-end electronics with asynchronous readout that provides pixel position and time over threshold information. Finally, there is the category of CE65 (Circuit Exploratoire 65 nm) that consists of structures with 64×32 pixels and 15 μm pitch or

48 ×32 pixels with 25 µm pitch; they are provided with analog rolling shutter readout and are used mainly to study the pixel matrix uniformity.

2.1 Tests and results

The first tests have been performed on the APTS that has been realized in 2 output buffer versions: the first, called source follower (SF), gives direct access to front end amplitude; the second (OA) is equipped with a fast operational amplifier output buffer for better timing [8]. Effects of optimization process have been studied using a ^{55}Fe radioactive source, that emits an intense X-ray line at 5.9 keV (Mn K_α) and a weaker one at 6.5 keV (Mn K_β).

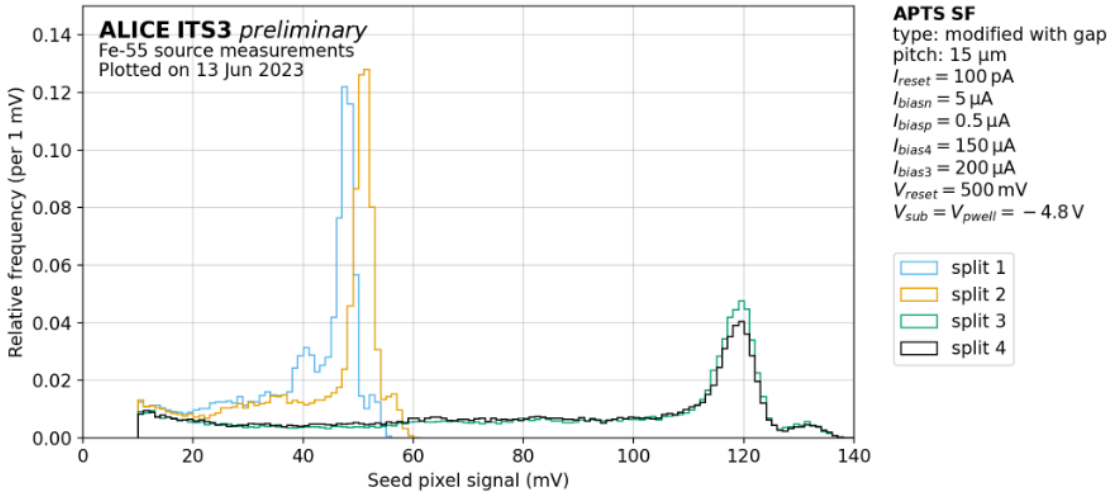

Figure 1: Spectrum of a ^{55}Fe radioactive source acquired with chips APTS (version SF) produced in the four splits planned for sensor optimization.

Figure 1 shows the signal provided by the seed pixel of a chip produced with the standard process (blue histogram) and after the consecutive adjustments of positive and negative wells [9]. It is clear that the last 2 splits, thanks to a smaller input node capacitance, provide a signal 3 times higher respect to the default process, so the 4th split has been chosen for next submissions.

Effects of pixel optimization are shown in Fig. 2, that reports the signal produced by the seed pixel during measurements performed with the 3 different types of pixels realized during the 4th split (the optimized one). Collected spectra show that *standard* chips are characterized by an important effect of charge sharing between the seed pixel and neighbouring ones while going to diodes *modified* and *modified with gap* this effect is strongly suppressed resulting in a sharp peak at the Mn K_α energy. This result has been confirmed for all the pixel pitches produced (10, 15, 20 and 25 µm); in particular the *standard* type shows a small peak efficiency especially for increasing pitch, while pixels *modified with gap* concentrates charge sufficiently to remain efficient also for the larger pitch. Detection efficiency of the sensors has been tested using a beam of 120 GeV/*c* hadrons delivered by the Super Proton Synchrotron of CERN. The results are reported in Fig. 3, where dashed lines represent the efficiency obtained with the chips *modified*, while the continuous lines represent the type *modified with gap*, that has the better behaviour, giving an efficiency higher than 99% especially for the larger pitch. In particular, the optimized charge collection of chips *modified with gap* lead to a cluster size limited mainly to 1 (from 58% of events for 10 µm pitch to 71% for 25 µm one) or 2 (from 26% for 25 µm pitch to 33% for 10 µm one)

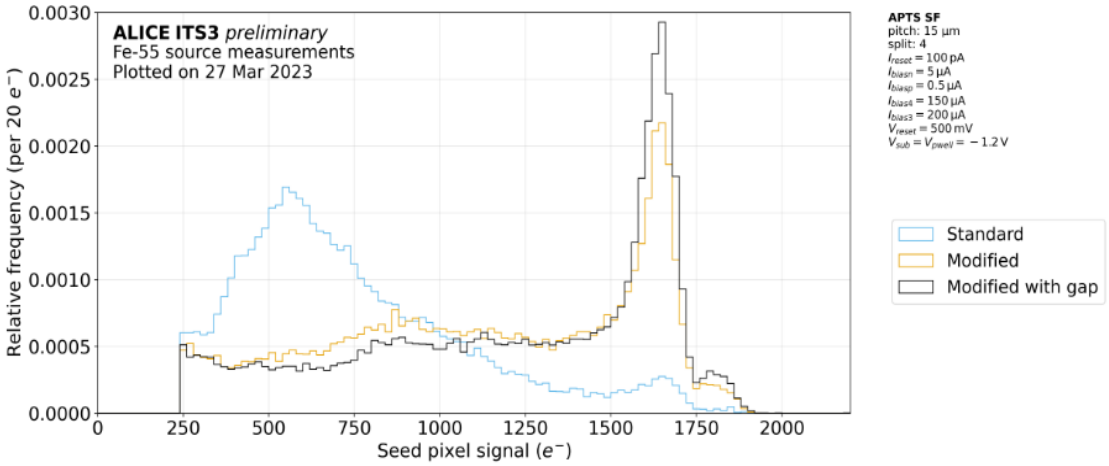

Figure 2: Charge collected by the seed pixel during ^{55}Fe source measurements performed using APTS (SF version) with the 3 different types of pixels realized in the 4th split (the optimized one).

pixels for all the pitches.

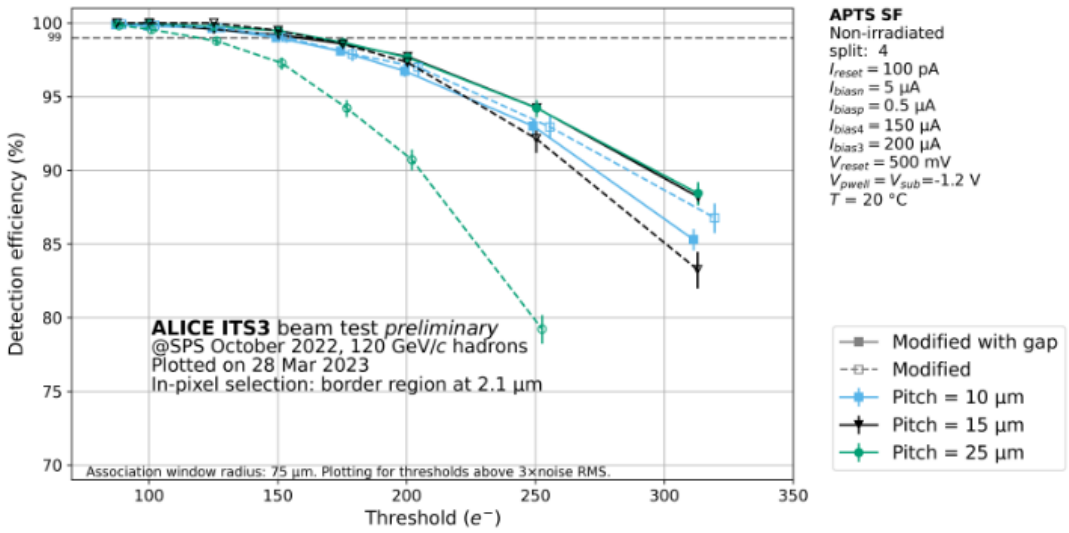

Figure 3: Detection efficiency of APTS SF obtained in the first beam tests with 120 GeV/*c* hadrons delivered by the Super Proton Synchrotron of CERN. Dashed lines refer to the chips *modified* while the continuous lines represent the type *modified with gap*.

Similar results have been obtained also with the APTS-OPAMP, a version of the chip equipped with a fast operational amplifier for a better timing; the time interval between signals provided by 2 identical chips (version *modified with gap*) placed one after the other in front of the hadron beam has a standard deviation of the order of 100 ps, confirming the prediction of simulation that collection time is lower than 1 ns, while for the *standard* pixels the evaluation is 30 times higher.

After the charge collection, diode signal is processed by in-pixel full-digital front-end electronics, that has been developed with the Digital Pixel Test Structures (DPTS). These structures, that have been realized in the pixel version *modified with gap*, are equipped with an asynchronous digital readout system and also provide time over threshold information pixel by pixel. Figure 4 shows the spectrum stored with the ^{55}Fe radioactive source; the untreated spectrum

(blue hist.) shows a poor resolution but after a suitable calibration of time over threshold, that is applied to account for the variation in the pixel-to-pixel response, the resolution improves until in the spectrum (yellow hist.) the small Mn-K$_\alpha$ and Mn-K$_\beta$ emission peaks are clearly resolved.

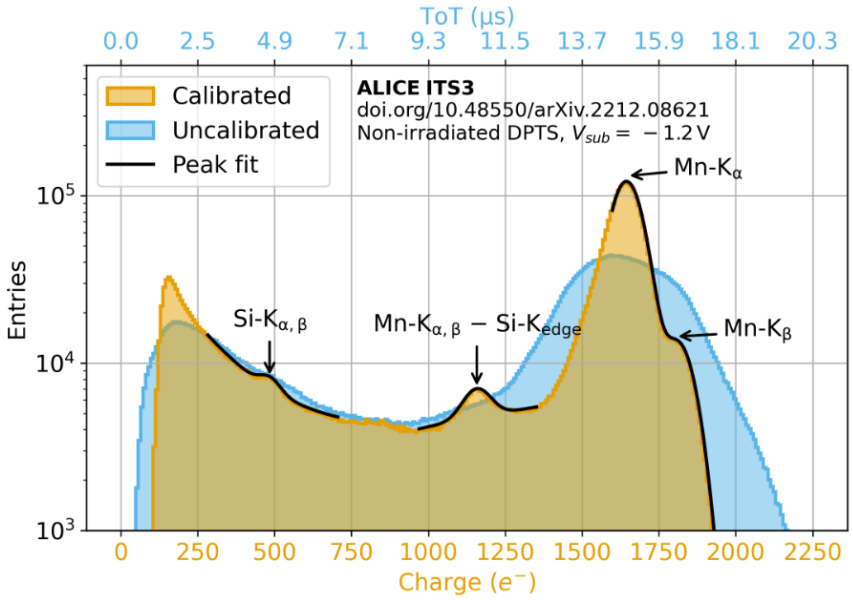

Figure 4: Spectrum of a ^{55}Fe radioactive source collected with a DPTS. The blue histogram represents the untreated spectrum, while the yellow one represents the spectrum obtained after a suitable pixel-to-pixel calibration of *time over threshold* provided by this version of chip.

Another important feature of this technology is the non-ionizing energy loss (NIEL) radiation hardness, that has been addressed during 120 GeV/*c* hadrons beam tests using samples previously irradiated up to 10^{15} 1 MeV n_{eq} / cm^2; after this huge irradiation level (above the value expected at ALICE in Run 4), chips *modified with gap* preserve a detection performance of 99% (Fig. 5).

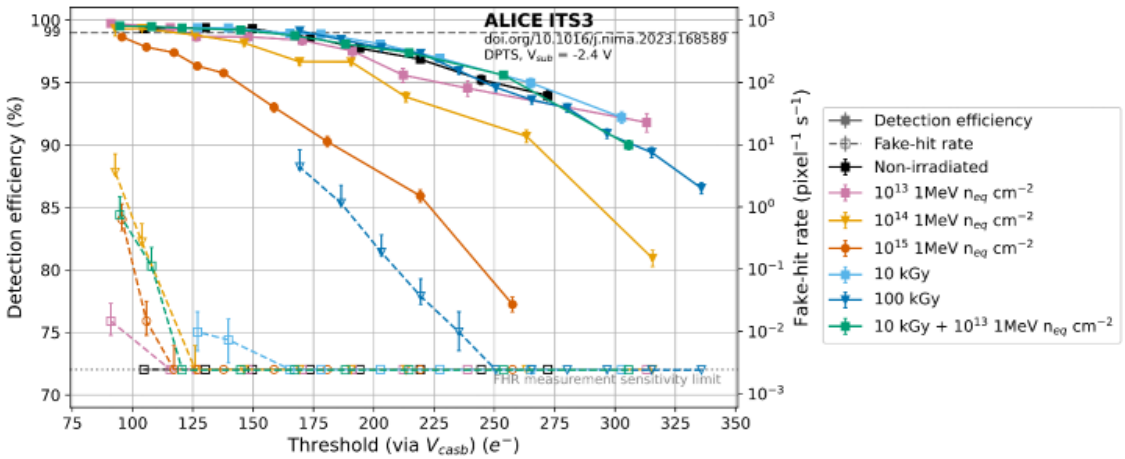

Figure 5: Detection efficiency (filled symbols) and fake-hit rate (open symbols) obtained with DPTS (15µm pixel pitch) during beam tests with 10 GeV/*c* hadrons at different values of irradiation dose.

3. Conclusion and outlook

This work presented the performance studies on the first structures realized in 65 nm CMOS process for the upgrade of ALICE Inner tracking system. A number of chip variants, differing in

layout, doping profile, and circuitry have been produced and tested with excellent results. Sensors have been gradually optimized achieving a high charge collection efficiency and a strong suppression of the charge sharing between neighbouring pixels for all the pitch dimensions. The detection efficiency of charged hadrons is 99% and the charge collection time resolution was estimated around 100 ps. The in-pixel full-digital front-end electronics ensures low noise operation and give DPTS an outstanding spatial resolution: during beam tests with 10 GeV/*c* hadrons it settles on 4 µm while the average cluster size is 1.2 pixel. Regarding power consumption, the bias current of DPTS can be lowered up to 20 nA per pixel without losing performance, also after radiation damage: all the characteristics have been verified at 10^{13} 1 MeV n_{eq}/cm^2, that is the irradiation level forecasted for the ITS3 operation, but the operability is maintained up to 10^{15} 1 MeV n_{eq}/cm^2, making these devices even more appealing in view of further developments towards ALICE-3 [10].

In conclusion the 65 nm CMOS technology for detector designs has been qualified and is ready for next steps that are stitching of chips to produce sensors much larger than the design reticle [3] and bending of large sensors to obtain cylindrical wafer-scale sensors [11].

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